USER'S MANUAL

IMB711

ATX Motherboard with LGA4677 Socket 5th/4th Gen Intel® Xeon® Scalable Processors, Intel® C741, 4 PCIe x16 slots, NVMe and OpenBMC

AXIOMTEK

www.axiomtek.com

Disclaimers

This manual has been carefully checked and believed to contain accurate information. Axiomtek Co., Ltd. assumes no responsibility for any infringements of patents or any third party's rights, and any liability arising from such use.

Axiomtek does not warrant or assume any legal liability or responsibility for the accuracy, completeness or usefulness of any information in this document. Axiomtek does not make any commitment to update the information in this manual.

Axiomtek reserves the right to change or revise this document and/or product at any time without notice.

No part of this document may be reproduced, stored in a retrieval system, or transmitted, in any form or by any means, electronic, mechanical, photocopying, recording, or otherwise, without the prior written permission of Axiomtek Co., Ltd.

CAUTION

Wrong type of batteries may cause explosion. It is recommended that users only replace with the same or equivalent type of batteries as suggested by the manufacturer once properly disposing of any used ones.

November 2025, Version A1

Printed in Taiwan

ESD Precautions

Computer boards have integrated circuits sensitive to static electricity. To prevent chipsets from electrostatic discharge damage, please take care of the following jobs with precautions:

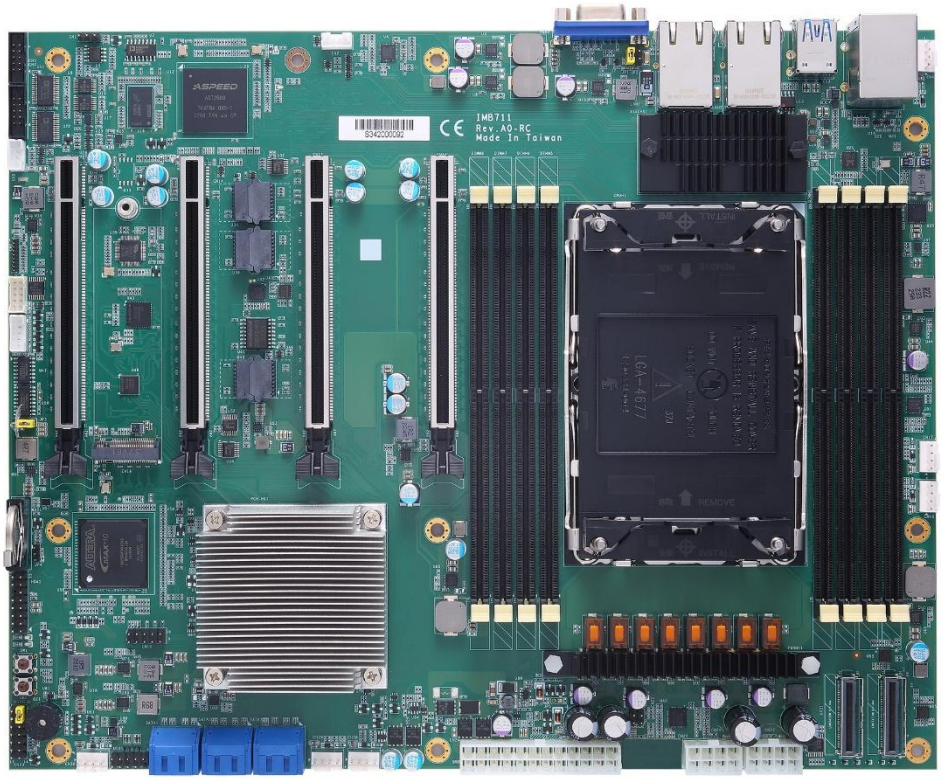
- Do not remove boards or integrated circuits from their anti-static packaging until you are ready to install them.
- Before holding the board or integrated circuit, touch an unpainted portion of the system unit chassis for a few seconds to discharge static electricity from your body.
- Wear a grounding wrist strap, available from most electronic component stores, when handling boards and components.

Trademarks Acknowledgments

Table of Contents

This page is intentionally left blank.

Section 1
Introduction



The IMB711 is an advanced ATX server board based on the 5th/4th Gen Intel® Xeon® Scalable processors in an LGA4677 socket and comes with an Intel® C741 chipset. Featuring enhanced computing power to deliver optimal computing and visual performance, the IMB711 motherboard is an ideal solution for developing medical AI and medical image processing applications ranging from deep learning AI, high-end inspection with AI and video streaming. To maximize expandability, the mother board comes with four PCIe x16 slots for multiple dual slots AI acceleration cards to deliver superior graphics performance, two 10 Gigabit LANs with Intel® Ethernet controller X550, one dedicated OpenBMC LAN port, M.2 M key 2280 and two MCIO for storage. It also supports Trusted Platform Module 2.0 (TPM 2.0) to ensure critical information security. Furthermore, the IMB711 meets the ESD protection requirements for medical fields and passes the Contact ±8KV / Air ±15KV test.

1.1 Features

- 5th/4th Gen Intel® Xeon® Scalable processors
- 8 x DDR5-5200 ECC RDIMM
- 4 x PCIe Gen5 x16 double-width slots
- Supports 2 Mini Cool Edge IO (MCIO) connectors with PCIe Gen5 x8
- Supports dual 10GbE LAN ports and 1 dedicated IPMI LAN port
- Supports TPM 2.0
- Supports redundant BIOS and BMC

1.2 Specifications

- **CPU**
  - LGA4677 socket (socket E) 5th/4th Gen Intel® Xeon® Scalable processors (Platinum, Gold, Silver and Bronze), up to 270W TDP

- **Chipset**
  - Intel® C741

- **BIOS**
  - AMI BIOS
  - Redundant BIOS (U48 Primary/U45 Secondary)

- **BMC**
  - Redundant BMC (U38 Primary/U34 Secondary)

- **System Memory**
  - 8 x R-DIMM sockets
  - Maximum 512GB DDR5 memory (max. 64GB per slot)
  - Supports 5200MHz
  - Supports the memory with ECC function

- **Onboard Multi I/O**
  - 2 x RS-232 (internal I/O)
  - 1 x SMBus
  - 1 x PMBus
  - 1 x IPMB
  - 1 x DIO 8-channel TTL

- **USB Interface**
  - 4 x USB 3.2 Gen1
  - 2 x internal USB 2.0

- **Ethernet**
  - 2 x 10Gbps Ethernet (Intel® X550-AT2)
  - 1 x Dedicated IPMI LAN port (Realtek RTL8211F)

- **Storage**
  - 6 x SATAIII with RAID 0/1/5/10
  - 1 x M.2 2280 Key M with PCIe Gen4 x4 signal for NVMe SSD
  - 1 x MCIO (PCIe Gen5 x8) for 2 x NVMe SSD

- **Audio**
  - Supports HD audio interface as a 2x8 pin header

- **Display**
  - 1 x 15-pin D-Sub as VGA connector. Resolution max. up to 1920x1200 @60Hz
  - AST2600

- **Expansion Interface**
  - Slot 1,2,3: PCIe x16 (Gen5 x16)
  - Slot 4: PCIe x16 (Gen5 x8)
  - Slot 5: NVMe M.2 2280 Key M (PCIe Gen4 x4)

- **Power Input**
  - 1 x 24-pin ATX power input connector
  - 2 x 12V ATX power input connector for CPU Power

- **Operating Temperature**
  - 0°C ~ 40°C (+32°F to +104°F), depends on cooler solution

- **Storage Temperature**
  - -10°C ~ 85°C

- **Operating Humidity**
  - 10% to 95% relative humidity, non-condensing

- **Dimensions**
  - 305 x 244mm (12” x 9.6”)

- **EMC Safety**
  - Contact ±8KV; Air ±15KV

1.3 Packing list

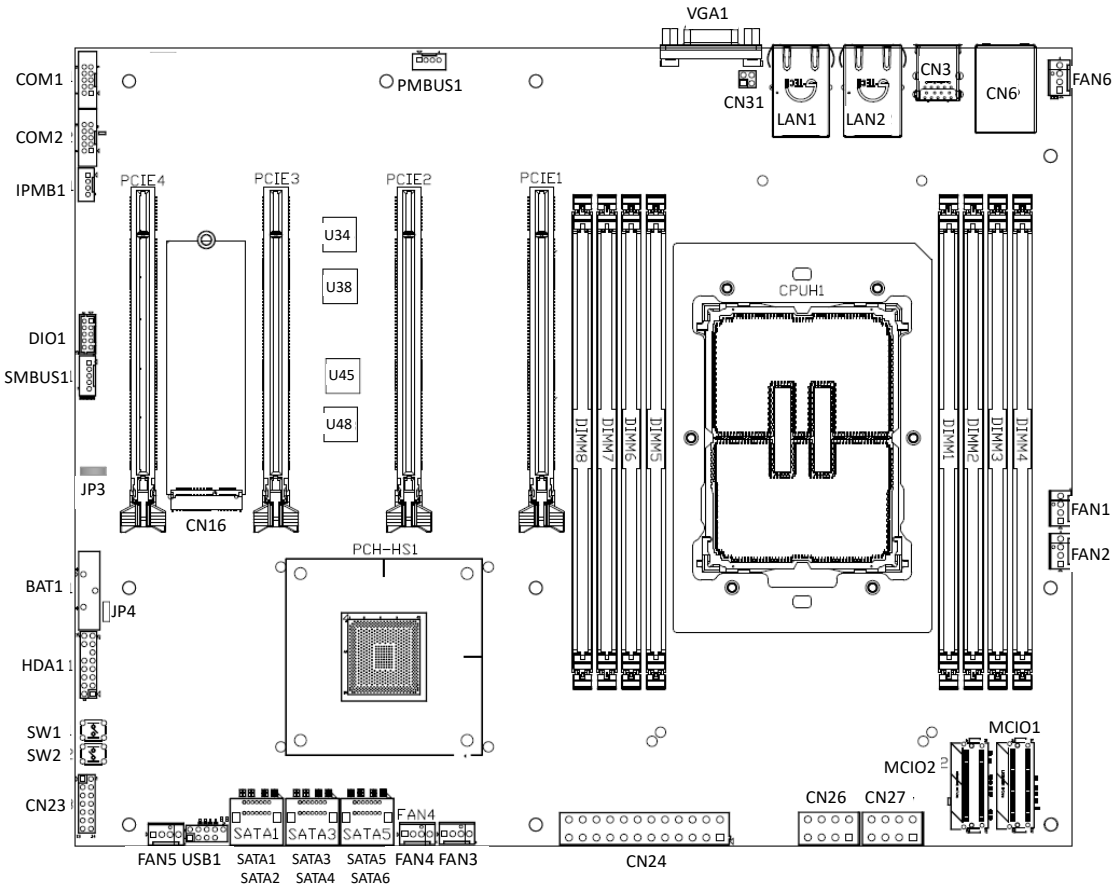
- **Bulk packing**
  - 1 x Motherboard
  - 1 x I/O bracket
  - 1 x LGA4677 CPU carrier - E1A
  - 1 x LGA4677 CPU carrier - E1B

- **Gift box**
  - 1 x Motherboard
  - 1 x I/O bracket
  - 1 x LGA4677 CPU carrier - E1A
  - 1 x LGA4677 CPU carrier - E1B

This page is intentionally left blank.

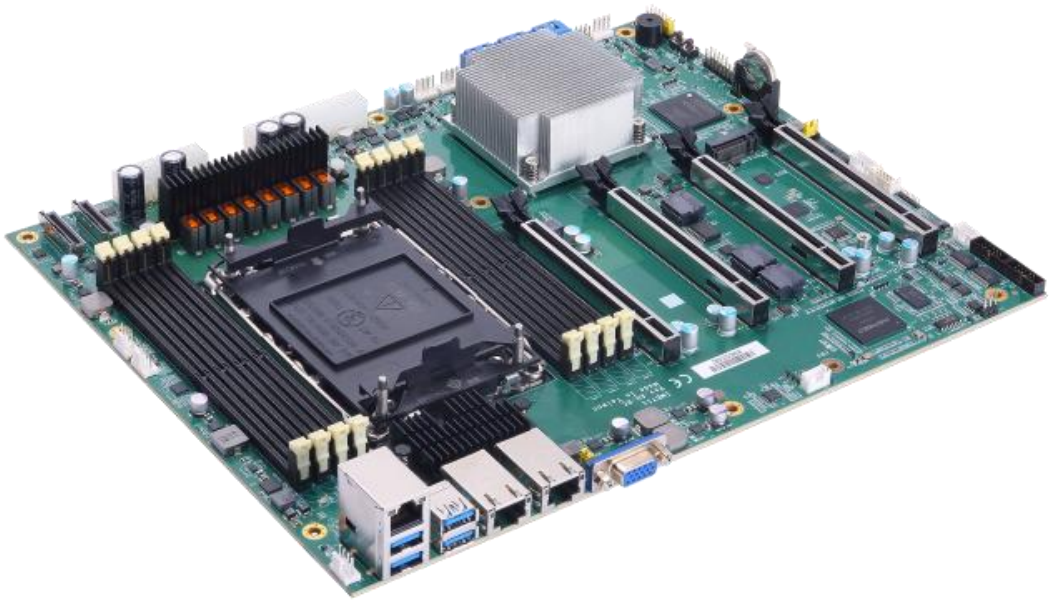
Section 2
Board and Pin Assignments

2.1 Board Layout

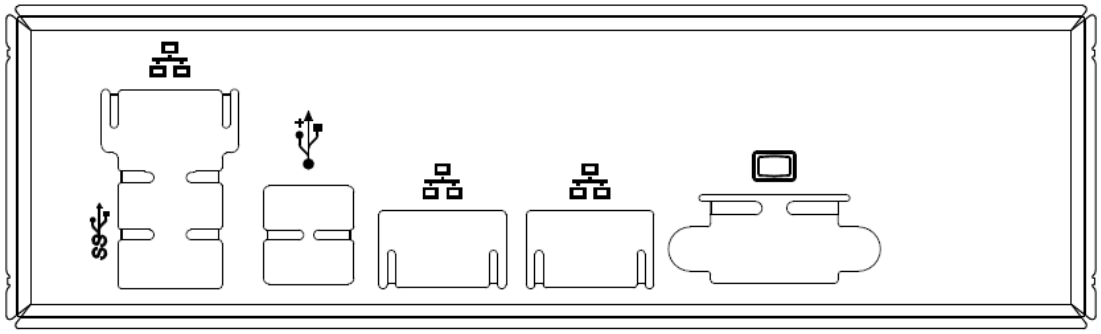


Top side

2.2 Rear I/O

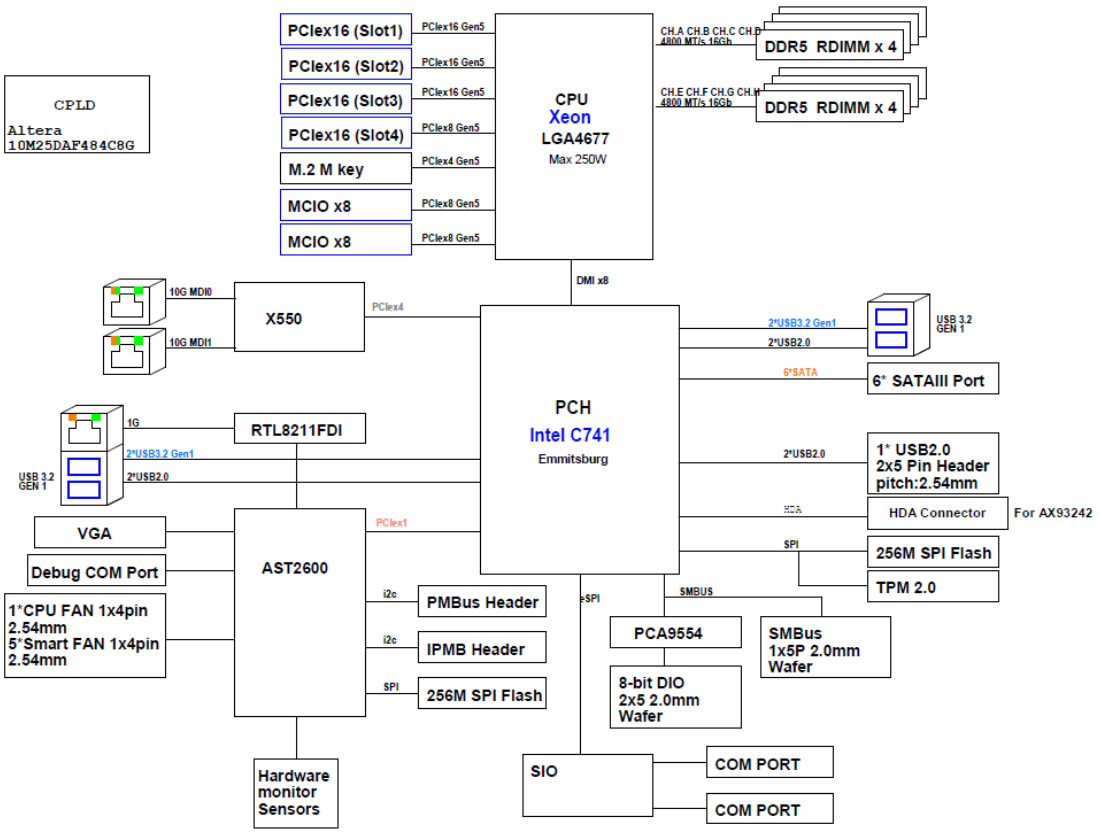


I/O side



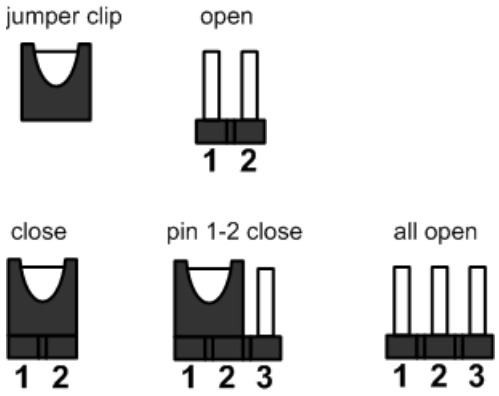
I/O bracket

2.3 Block Diagram



2.4 Jumper Settings

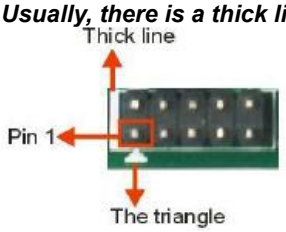
Pin description
Jumper is a small component consisting of jumper clip and jumper pins. Install jumper clip on 2 jumper pins to close. And remove jumper clip from 2 jumper pins to open. Below illustration shows how to set up jumper.



Note

To identify the first pin of a header or jumper, please refer to the following information:

- ***Usually, there is a thick line or a triangle near the header or jumper pin 1.***



- ***A square pad, which you can find on the back of the motherboard, is usually used for pin 1.***

Before applying power to the IMB711, make sure all of the jumpers are in factory default position. Below you can find a summary table of all jumpers and onboard default settings.

Note

Turn off power before changing any default jumper settings.

Jumper	Description	Setting
JP3	ATX power mode (AT mode BOM option) Default: ATX mode	Location reserved, no jumper
JP4	Clear CMOS Default: Normal Operation	1-2 Close

2.4.1 ATX/AT mode (JP3)_BOM option

This 3x1-pin jumper (pitch=2.54mm) allows you to select AT or ATX power mode.

Function	Setting
AT mode (Default)	1-2 close
ATX mode	2-3 close

**BOM Option, location reserved only, no jumper on board*

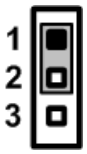
2.4.2 Clear CMOS (JP4)

This 3x1-pin jumper (pitch=2.54mm) allows you to clear Real Time Clock (RTC) RAM in CMOS. You can clear the CMOS memory of date, time, and system setup parameters by erasing the CMOS RTC RAM data. The onboard button cell battery powers the RAM data in CMOS, which stores system setup information such as system passwords.

To erase the RTC RAM:

1. Turn OFF the computer and unplug the power cord.
2. Remove the onboard battery.
3. Move the jumper clip from pins 1-2 (default) to pins 2-3. Keep the clip on pins 2-3 for about 5~10 seconds, then move the clip back to pins 1-2.
4. Re-install the battery.
5. Plug the power cord and turn ON the computer.
6. Hold down the <Del> key during the boot process and enter BIOS setup to re-enter data.

Function	Setting
Normal operation (Default)	1-2 close
Clear CMOS	2-3 close



2.5 Connectors and Switch Buttons

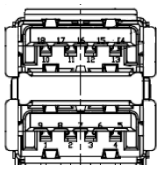
Signals go to other parts of the system through connectors. Loose or improper connection might cause problems, Make sure all connectors are properly and firmly connected. Here is a summary table showing the connectors on the hardware.

Connector	Description
CN3	USB 3.2 Gen1 Port
CN6	BMC LAN + USB 3.2 Gen1 Port
CN16	M.2 Key M Connector
CN23	Front Panel Header
CN24	ATX Power Connector
CN26~CN27	ATX CPU 12V Power Connectors
CN31	LAN Active LED Connector
COM1~COM2	COM1 and COM2 Box Headers
DIO1	GPIO Connector
LAN1~LAN2	Ethernet Ports
VGA1	VGA Connector
BAT1	RTC Battery Connector
HDA1	Audio Header (for AX93242)
USB1	USB 2.0 Header
PMBUS1	PMBus Connector
IPMB1	IPMB Connector
SMBUS1	SMBus Connector
FAN1~FAN6	Fan Headers
SATA1~SATA6	SATA 3.0 Connectors
MCIO1~MCIO2	MCIO Connectors
PCIE1~PCIE3	PCI-Express x16 Connectors (Gen5 x16)
PCIE4	PCI-Express x16 Connector (Gen5 x8)
DIMM1~DIMM8	DDR5 RDIMM Connectors
SW1	Reset Button
SW2	Power Button

2.5.1 USB 3.2 Gen1 Port (CN3)

The motherboard has two Universal Serial Bus (compliant with USB 3.2 Gen1) connectors on the rear I/O for installing USB peripherals such as a keyboard, mouse, scanner, etc.

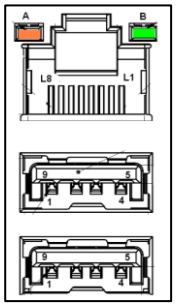
Pin	Signal	Pin	Signal
1	USB3_POWER	2	USB1 -
3	USB1 +	4	GND
5	USB3_SSRX1-	6	USB3_SSRX1+
7	GND	8	USB3_SSTX1-
9	USB3_SSTX1+	10	USB3_POWER
11	USB2 -	12	USB2 +
13	GND	14	USB3_SSRX2-
15	USB3_SSRX2+	16	GND
17	USB3_SSTX2-	18	USB3_SSTX2+



2.5.2 BMC LAN + USB 3.2 Gen 1 Port (CN6)

The motherboard has one high-performance, plug-and-play, BMC-dedicated RJ-45 Ethernet interface, which is fully compliant with the IEEE 802.3 standard. Connection can be established by plugging one end of the Ethernet cable into this connector and the other end to a 1000/100 Base-T hub.

Pin	LAN Signal	Pin	LAN Signal
L1	Tx+ (Data transmission positive)	L2	Tx- (Data transmission negative)
L3	Rx+ (Data reception positive)	L4	RJ-1 (For 1000 Base-T only)
L5	RJ-1 (For 1000 Base-T only)	L6	Rx- (Data reception negative)
L7	RJ-1 (For 1000 Base-T only)	L8	RJ-1 (For 1000 Base-T only)
A	100 LAN LED (Green) / 1000 LAN LED (Orange)	B	Active LED



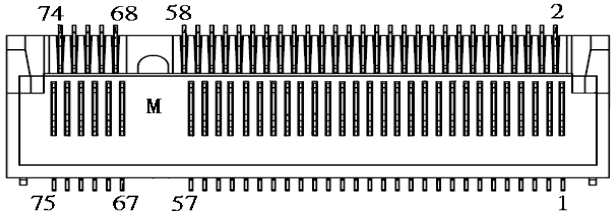
Pin	USB Signal	Pin	USB Signal
1	USB3_POWER	2	USB1 -
3	USB1 +	4	GND
5	USB3_SSRX1-	6	USB3_SSRX1+
7	GND	8	USB3_SSTX1-
9	USB3_SSTX1+		

Note

IPMI IP Address will shows in first screen under AMI logo when power on.

2.5.3 M.2 Key M Connector (CN16)

The motherboard has one M.2 2280 Key M slot with PCIe x4 signal for NVMe SSD storage.

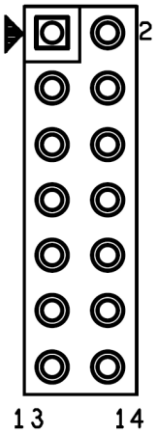


Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	GND	2	+3.3V	3	GND	4	+3.3V
5	PEX3_RX-	6	NC	7	PEX3_RX+	8	NC
9	GND	10	LED_1#	11	PEX3_TX-	12	+3.3V
13	PEX3_TX+	14	+3.3V	15	GND	16	+3.3V
17	PEX2_RX-	18	+3.3V	19	PEX2_RX+	20	NC
21	GND	22	NC	23	PEX2_TX-	24	NC
25	PEX2_TX+	26	NC	27	GND	28	NC
29	PEX1_RX-	30	NC	31	PEX1_RX+	32	NC
33	GND	34	NC	35	PEX1_TX-	36	NC
37	PEX1_TX+	38	M.2_DEVSLP	39	GND	40	NC
41	PEX0_RX-	42	NC	43	PEX0_RX+	44	NC
45	GND	46	NC	47	PEX0_TX-	48	NC
49	PEX0_TX+	50	PERST#	51	GND	52	CLKREQ#
53	PEX0_REFCLKn	54	PEWAKE#	55	PEX0_REFCLKp	56	NC
57	GND	58	NC	59	CONNECTOR Key M	60	CONNECTOR Key M
61	CONNECTOR Key M	62	CONNECTOR Key M	63	CONNECTOR Key M	64	CONNECTOR Key M
65	CONNECTOR Key M	66	CONNECTOR Key M	67	NC	68	NC
69	NC	70	+3.3V	71	GND	72	+3.3V
73	GND	74	+3.3V	75	GND		

2.5.4 Front Panel Header (CN23)

This is a 7x2-pin header (pitch=2.54mm) for front panel interface.

Pin	Signal
1	Power LED+
2	Onboard BMC HEALTH LED+
3	GND
4	Onboard BMC HEALTH LED-
5	Power LED-
6	N/C
7	N/C
8	+5V
9	PWR Switch-
10	PWR Switch+
11	RESET-
12	RESET+
13	HDD/SSD LED-
14	HDD/SSD LED+



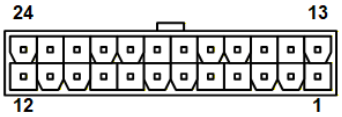
2.5.5 ATX Power Connectors (CN24, CN26 and CN27)

Steady and sufficient power can be supplied to all components on the motherboard by connecting the power connector. Please make sure all components and devices are properly installed before connecting the power connector.

An external power supply plug fits into CN24/26/27 in only one orientation. Properly press down the power supply plug until it completely and firmly fits into the connector. Loose connection may cause system instability.

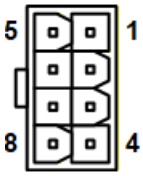
CN24 (24-pin ATX power input connector):

Pin	Signal	Pin	Signal
1	3.3V	13	3.3V
2	3.3V	14	-12V
3	GND	15	GND
4	+5V	16	PS_ON
5	GND	17	GND
6	+5V	18	GND
7	GND	19	GND
8	PWR OK	20	-5V
9	5VSB	21	+5V
10	+12V	22	+5V
11	+12V	23	+5V
12	3.3V	24	GND



CN26/CN27 (8-pin ATX CPU 12V power input connector):

Pin	Signal	Pin	Signal
1	GND	5	+12V
2	GND	6	+12V
3	GND	7	+12V
4	GND	8	+12V



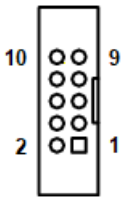
2.5.6 LAN Active LED Connector (CN31)

Function	Setting
LAN1 Active LED	1 LAN1 LED+ 2 LAN1 LED-
LAN2 Active LED	3 LAN2 LED+ 4 LAN2 LED-

2.5.7 COM Box Headers (COM1 and COM2)

The motherboard has two 5x2-pin headers for COM1 and COM2 serial port interfaces.

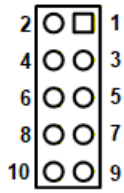
Pin	Signal	Pin	Signal
1	DCD#	2	DSR#
3	RXD#	4	RTS#
5	TXD#	6	CTS#
7	DTR#	8	RI#
9	GND	10	N/C



2.5.8 GPIO Connector (DIO1)

This is a 5x2-pin header (pitch=2.00mm) for digital I/O interface.

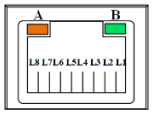
Pin	Signal	Pin	Signal
1	DIO1	2	DIO8
3	DIO2	4	DIO7
5	DIO3	6	DIO6
7	DIO4	8	DIO5
9	NA	10	GND



2.5.9 Ethernet Ports (LAN1 and LAN2)

The motherboard has two Intel® X550-AT2 RJ-45 10GbE Ethernet ports. Connection can be established by plugging one end of the Ethernet cable into this connector and the other end to a 10GbE/1GbE/100 M/s Base-T.

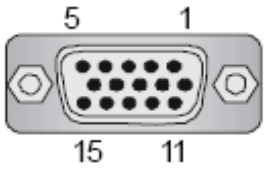
Pin	LAN Signal	Pin	LAN Signal
L1	Tx+ (Data transmission positive)	L2	Tx- (Data transmission negative)
L3	Rx+ (Data reception positive)	L4	RJ-1 (For 10GbE/1GbE Base-T)
L5	RJ-1 (For 10GbE/1GbE Base-T)	L6	Rx- (Data reception negative)
L7	RJ-1 (For 10GbE/1GbE Base-T)	L8	RJ-1(For 10GbE/1GbE Base-T)
A	1GbE LAN LED (Orange) / 10GbE LAN LED (Green)	B	Active LED(Green)



2.5.10 VGA Connector (VGA1)

The 15-pin D-Sub connector is commonly used for VGA display.

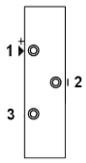
Pin	Signal	Pin	Signal
1	Red	2	Green
3	Blue	4	NC
5	GND	6	GND
7	GND	8	GND
9	VCC	10	GND
11	NC	12	DDC DATA
13	Horizontal Sync	14	Vertical Sync
15	DDC CLK		



2.5.11 RTC Battery Connector (BAT1)

The Real-Time battery interface is available through a 3-pin connector.

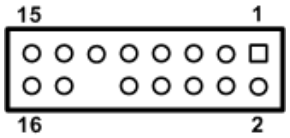
Pin	Signal
1	CR2032+
2	CR2032-
3	NC



2.5.12 Audio Header (HDA1)

This is a 2x8-pin header for connecting an external HD Audio board (AX93242).

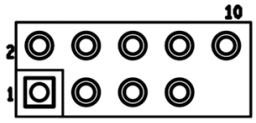
Pin	Signal	Pin	Signal
1	BCLK	2	GND
3	RST#	4	N.C
5	SYNC	6	GND
7	SDO	8	+3.3S
9	SDIO	10	+12VS
11	N.C	12	
13	N.C	14	N.C
15	N.C	16	GND



2.5.13 USB 2.0 Header (USB1)

This is a 2x5-pin (pin 9 cut) internal header for connecting USB 2.0 compliant peripheral devices.

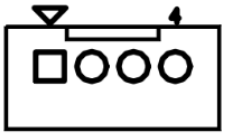
Pin	Signal
1	VBUS
2	VBUS
3	USB_4-
4	USB_5-
5	USB_4+
6	USB_5+
7	GND
8	GND
9	
10	GND



2.5.14 PMBus Connector (PMBUS1)

The Power System Management Bus connector monitors the power supply, system temperatures and fan.

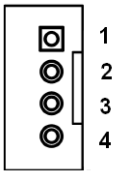
Pin	Signal
1	Clock
2	Data
3	PMBus Alert
4	GND



2.5.15 IPMB Connector (IPMB1)

The IPMB interface is available through a 4-pin connector.

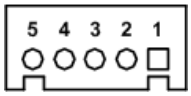
Pin	Signal
1	IPMB Clock
2	GND
3	IPMB Data
4	+5V



2.5.16 SMBus Connector (SMBUS1)

This is a 5x1-pin connector (pitch=2.00mm) for SMBus (System Management Bus) interface.

Pin	Signal	Pin	Signal
1	SMB_SCL	2	N/C
3	GND	4	SMB_SDA
5	+5V		



2.5.17 Fan Headers (FAN1~FAN6)

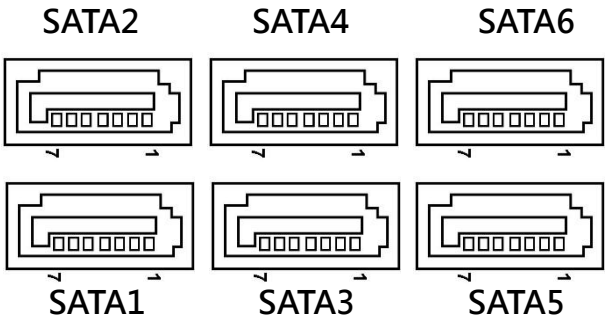
This motherboard has six 4x1-pin fan headers (pitch=2.54mm) for CPU and system fan connections. For fan speed configuration options, please refer to the OpenBMC website.

Pin	Signal
1	GND
2	+12V
3	FAN Speed Detection
4	FAN Speed Control (Smart FAN Control)

2.5.18 SATA 3.0 Connectors (SATA1~SATA6)

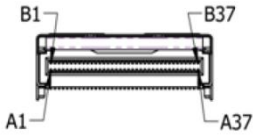
These Serial ATA (SATA) connectors support SATA 3.0 devices with data transfer rates of up to 6.0 Gb/s. SATA is a computer bus interface used to connect storage devices such as hard disk drives and solid-state drives. Each SATA port supports RAID 0, 1, 5, and 10 configurations.

Pin	Signal
1	GND
2	SATA_TX+
3	SATA_TX-
4	GND
5	SATA_RX-
6	SATA_RX+
7	GND



2.5.19 MCIO Connector (MCIO1, MCIO2)

The motherboard has one MCIO connector for 2 x NVMe SSD storage with PCIe x4 signal.



Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A1	GND	A20	RX4P	B1	GND	B20	TX4P
A2	RX0P	A21	RX4N	B2	TX0P	B21	TX4N
A3	RX0N	A22	GND	B3	TX0N	B22	GND
A4	GND	A23	RX5P	B4	GND	B23	TX5P
A5	RX1P	A24	RX5N	B5	TX1P	B24	TX5N
A6	RX1N	A25	GND	B6	TX1N	B25	GND
A7	GND	A26	GND	B7	GND	B26	SMB2_CLK
A8	GND	A27	WAKE#	B8	SMB1_CLK	B27	SMB2_DATA
A9	WAKE#	A28	GND	B9	SMB1_DATA	B28	GND
A10	GND	A29	CLK2_P	B10	GND	B29	PERST2
A11	CLK1_P	A30	CLK2_N	B11	PERST1	B30	GND
A12	CLK1_N	A31	GND	B12	GND	B31	GND
A13	GND	A32	RX6P	B13	GND	B32	TX6P
A14	RX2P	A33	RX6N	B14	TX2P	B33	TX6N
A15	RX2N	A34	GND	B15	TX2N	B34	GND
A16	GND	A35	RX7P	B16	GND	B35	TX7P
A17	RX3P	A36	RX7N	B17	TX3P	B36	TX7N
A18	RX3N	A37	GND	B18	TX3N	B37	GND
A19	GND			B19	GND		

2.5.20 Switch Buttons (SW1 and SW2)

The motherboard has two onboard switches for power-on and reset functions.

Function	Location
Reset Button	SW1
Power Button	SW2

2.6 Hardware Installation

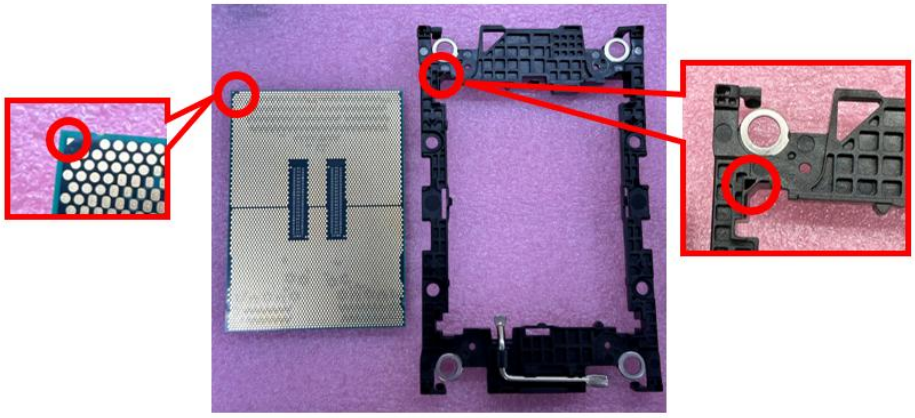
This section provides instructions for installing the IMB711 Series.

2.6.1 Installing the CPU

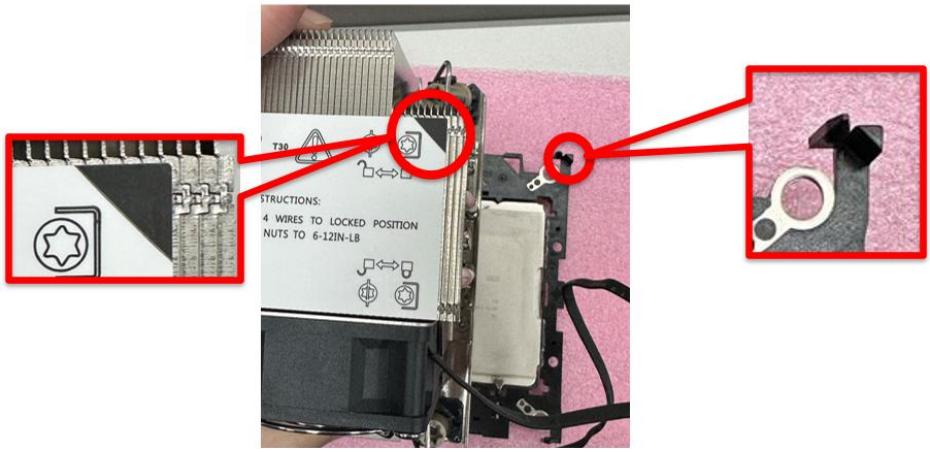
The LGA4677 processor socket comes with a cover to protect the processor. Please install the processor into the CPU socket step by step as illustrated below.

Step 1 Remove the socket protective covers. Press the load lever and release it from the retention tab.

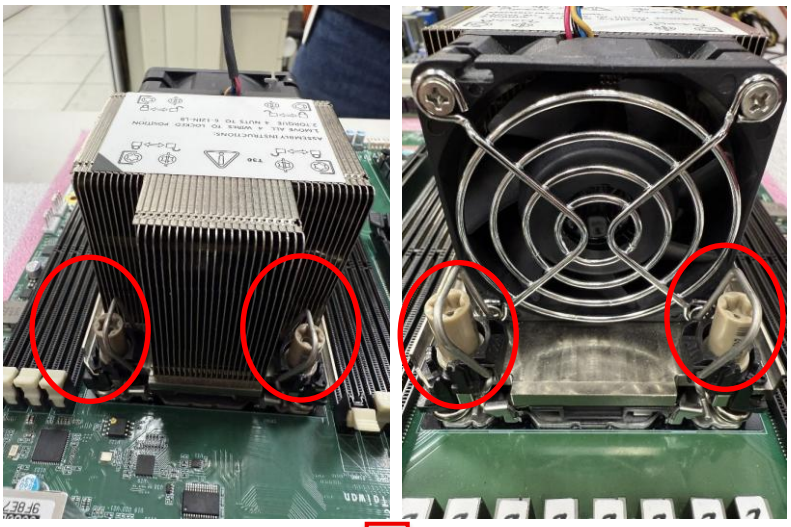
Step 2 Insert the CPU onto the CPU clip and align upper left pin mark on the CPU clip.



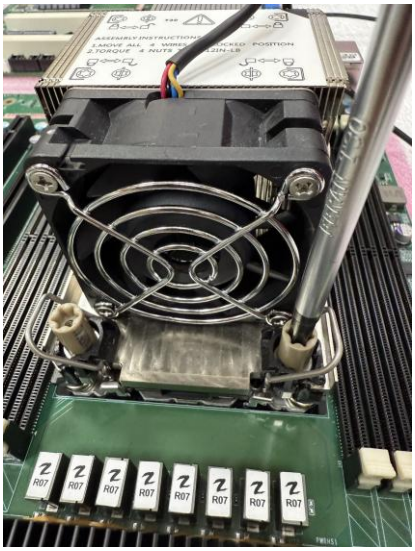
Step 3 Check the pin mark on the cooler and CPU clip and CPU.



Step 4 Latch four levers on the cooler.



Step 5 Use a T30 Torx screwdriver (8in-LBF) to tighten the screws on the cooler.



2.7 Memory Installation

The following table shows the recommended memory configuration, including the installed memory quantity. Different DIMM configurations can affect memory performance.

Channel		DIMM1	DIMM2	DIMM3	DIMM4	DIMM5	DIMM6	DIMM7	DIMM8
Quantity of Memory installed	1	V							
						V			
			V						
							V		
	2	V						V	
				V		V			
	4	V		V		V		V	
	6	V		V	V	V	V	V	
		V	V	V		V		V	V
			V	V	V	V	V		V
		V	V		V		V	V	V
	8	V	V	V	V	V	V	V	V

Section 3
Hardware Description

3.1 Microprocessors

The IMB711 series supports 5th/4th Gen Intel® Xeon® Scalable processors, which enable your system to operate under Windows® server 2022 and Linux environments. The system performance depends on the microprocessor. Make sure all correct settings are arranged for your microprocessor to prevent the CPU from damage.

Note

Caution: Ensure the power supply is turned off before installing the processor into the CPU socket.

3.2 BIOS

The IMB711 series uses AMI Plug and Play BIOS.

3.3 System Memory

The IMB711 supports eight DDR5 RDIMM sockets for maximum memory capacity up to 512GB of DDR5 RAMs. The memory module comes in sizes of 16GB, 32GB and 64GB.

This page is intentionally left blank.

Section 4
AMI BIOS Setup Utility

The AMI UEFI BIOS provides users with a built-in setup program to modify basic system configuration. All configured parameters are stored in a flash chip to save the setup information whenever the power is turned off. This section provides users with detailed description about how to set up basic system configuration through the AMI BIOS setup utility.

4.1 Starting

To enter the setup screens, follow the steps below:

1. Turn on the computer and press <Del> during the Power On Self Test (POST) to enter BIOS setup, otherwise, POST will continue with its test routines.
2. Once you enter the BIOS, the main BIOS setup menu displays. You can access the other setup screens from the main BIOS setup menu, such as the Advanced and Chipset menus.

Note

If your computer cannot boot after making and saving system changes with BIOS setup, you can restore BIOS optimal defaults by setting JP4 (see section 2.4.2).

It is strongly recommended that you should avoid changing the chipset's defaults. Both AMI and your system manufacturer have carefully set up these defaults that provide the best performance and reliability.

4.2 Navigation Keys

The BIOS setup/utility uses a key-based navigation system called hot keys. Most of the BIOS setup utility hot keys can be used at any time during the setup navigation process. These keys include <F1>, <F2>, <Enter>, <ESC>, <Arrow> keys, and so on.

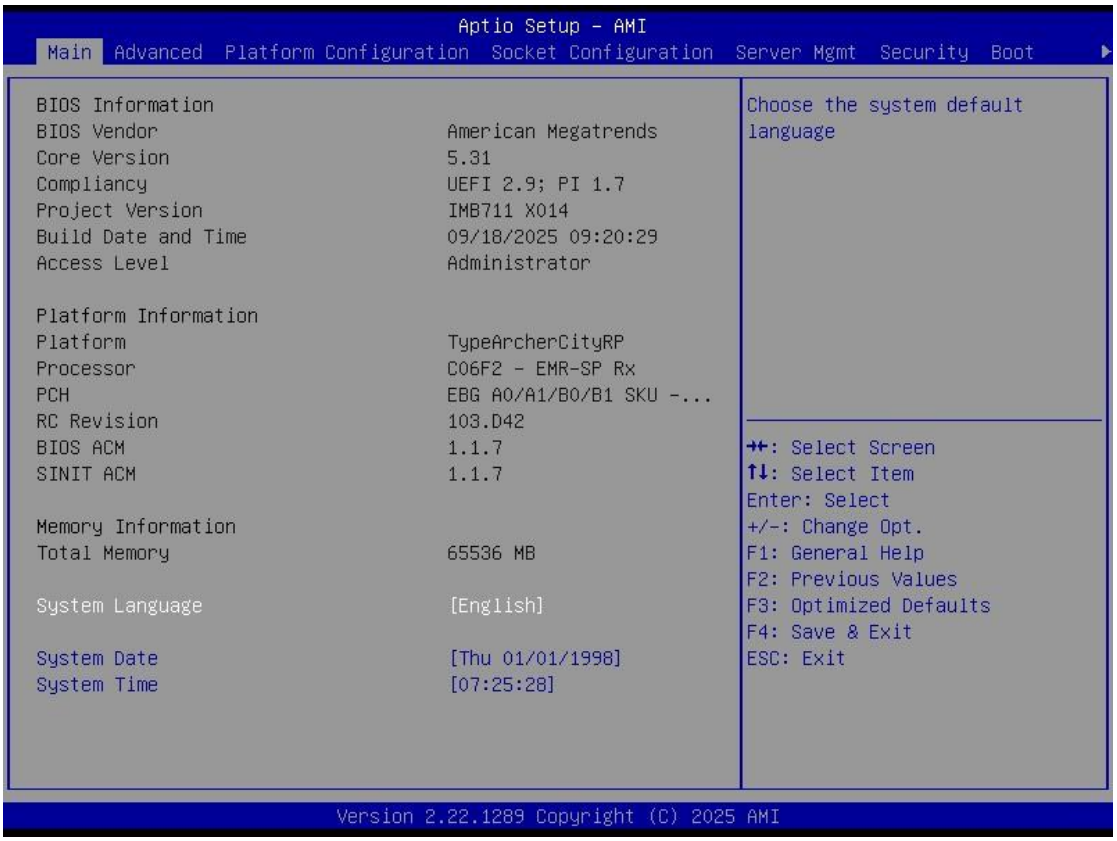
Note

Some of the navigation keys differ from one screen to another.

Hot Keys	Description
→← **Left/Right**	The Left and Right <Arrow> keys allow you to select a setup screen.
↑↓ **Up/Down**	The Up and Down <Arrow> keys allow you to select a setup screen or sub screen.
Enter	The <Enter> key allows you to display or change the setup option listed for a particular setup item. The <Enter> key can also allow you to display the setup sub screens.
+– Plus/Minus	The Plus and Minus <Arrow> keys allow you to change the field value of a particular setup item.
F1	The <F1> key allows you to display the General Help screen.
F2	The <F2> key allows you to Load Previous Values.
F3	The <F3> key allows you to Load Optimized Defaults.
F4	The <F4> key allows you to save any changes you have made and exit Setup. Press the <F4> key to save your changes.
Esc	The <Esc> key allows you to discard any changes you have made and exit the Setup. Press the <Esc> key to exit the setup without saving your changes.

4.3 Main Menu

When you first enter the setup utility, you will enter the Main setup screen. You can always return to the Main setup screen by selecting the Main tab. System Time/Date can be set up as described below. The Main BIOS setup screen is shown below.



BIOS/Platform/Memory Information
Display the BIOS/Platform/Memory information.

System Language
Choose the system default language.

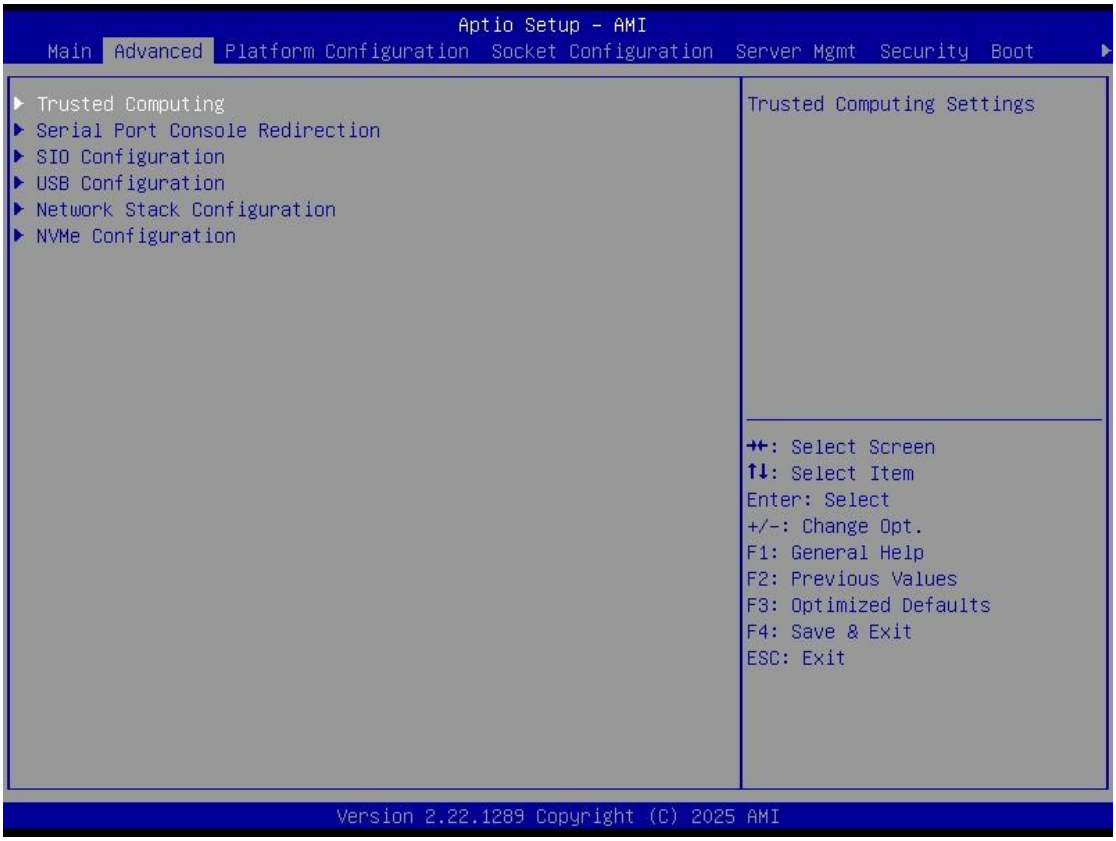
System Date/Time
Use this option to change the system time and date. Highlight System Time or System Date using the <Arrow> keys. Enter new values through the keyboard. Press the <Tab> key or the <Arrow> keys to move between fields. The date must be entered in MM/DD/YY format. The time is entered in HH:MM:SS format.

4.4 Advanced Menu

The Advanced menu also allows users to set configuration of the CPU and other system devices. You can select any of the items in the left frame of the screen to go to the sub menus:

- ► Trusted Computing
- ► Serial Port Console Redirection
- ► SIO Configuration
- ► USB Configuration
- ► Network Stack Configuration
- ► NVMe Configuration

For items marked with "►", please press <Enter> for more options.



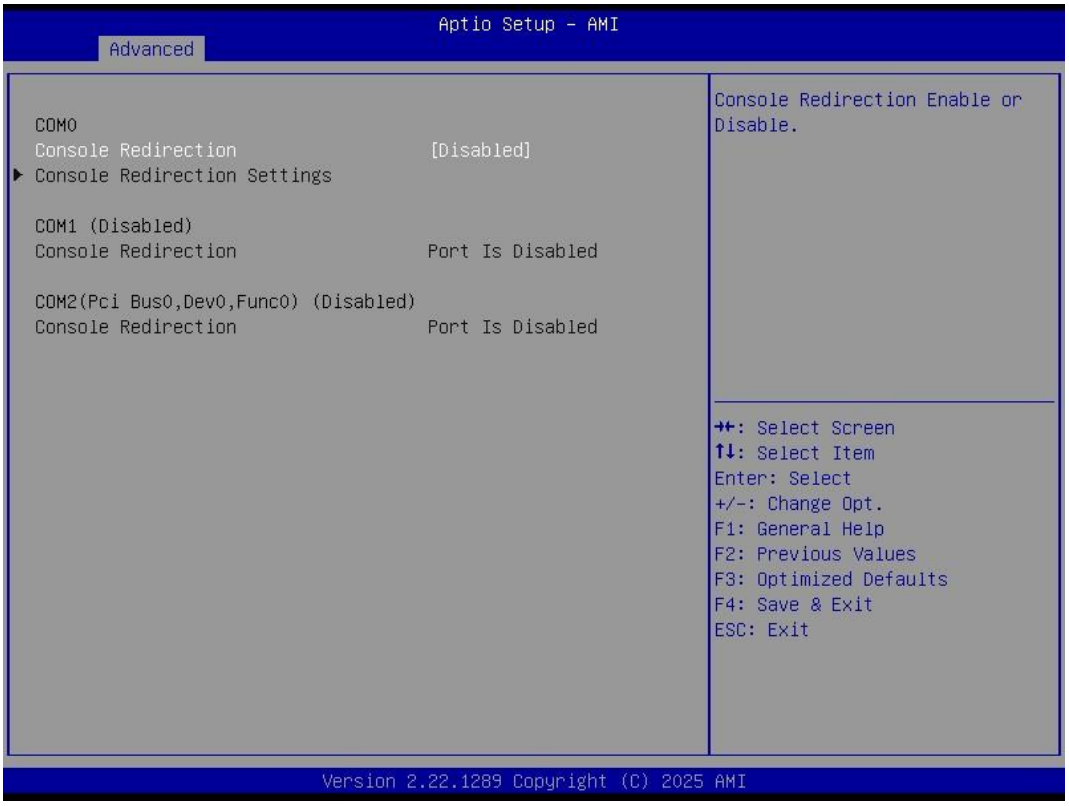
- **Trusted Computing**
  This screen provides function for specifying the TPM settings.

Security Device Support
Enable or disable BIOS support for security device, typically a TPM. When enabled (default setting), the BIOS initializes and makes the TPM available for use by the operating system and other system components. When disabled, the TPM is effectively hidden from the OS, and critical security functions, such as secure boot and disk encryption, may not function. Additionally, TCG EFI protocols and the INT1A interface, which are used for secure boot and other trusted computing tasks, will not be available.

Pending operation
Schedule an operation for the security device.
- None
- TPM Clear: Clear all data secured by TPM.

Note that your computer will reboot during restart in order to change State of Security Device.

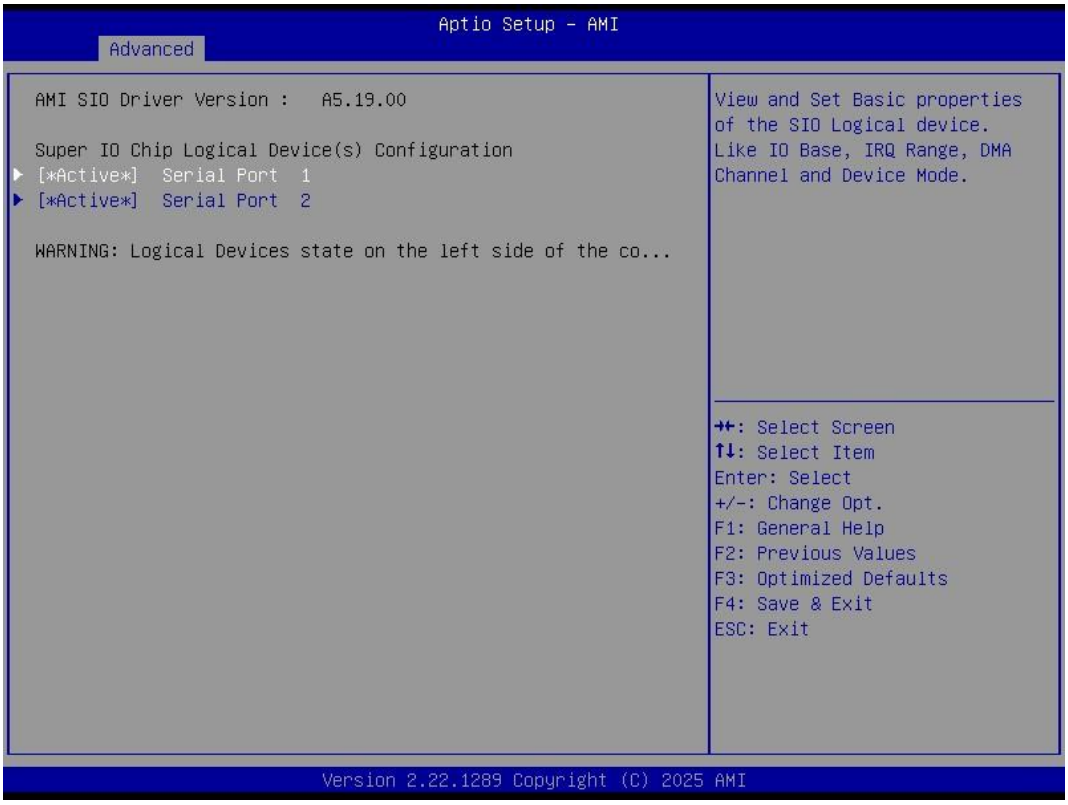
- **Serial Port Console Redirection**
  Enable or disable Console Redirection for BMC SOL function.
  You can use this screen to select options for Serial Port Console Redirection, and change the value of the selected option. A description of the selected item appears on the right side of the screen. For items marked with "►", please press <Enter> for more options.



Console Redirection
Enable or disable console redirection.

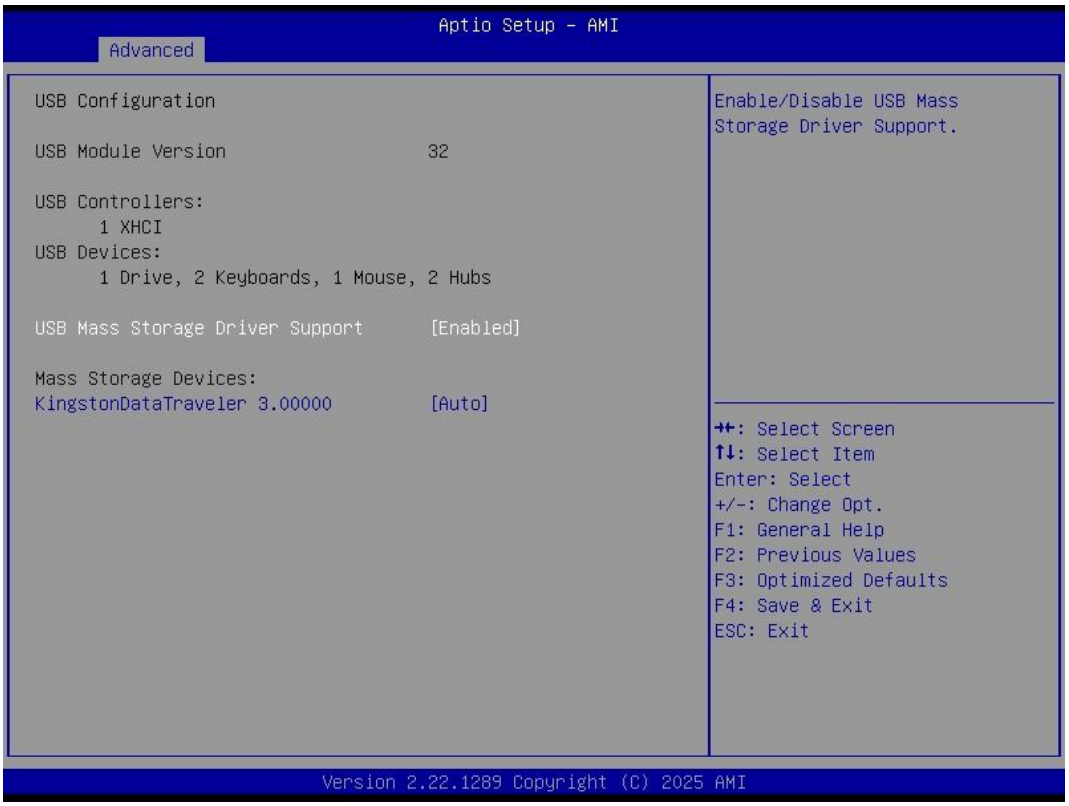
Console Redirection Settings
When enabled, the settings specify how the host computer and the remote computer (which the user is using) will exchange data. Both computers should have the same or compatible settings.

- **SIO Configuration**



Serial Port 1/Serial Port 2
View and set the parameters of the Super IO serial ports, including I/O base address, IRQ and port type.

- **USB Configuration**
  This screen shows USB configuration.

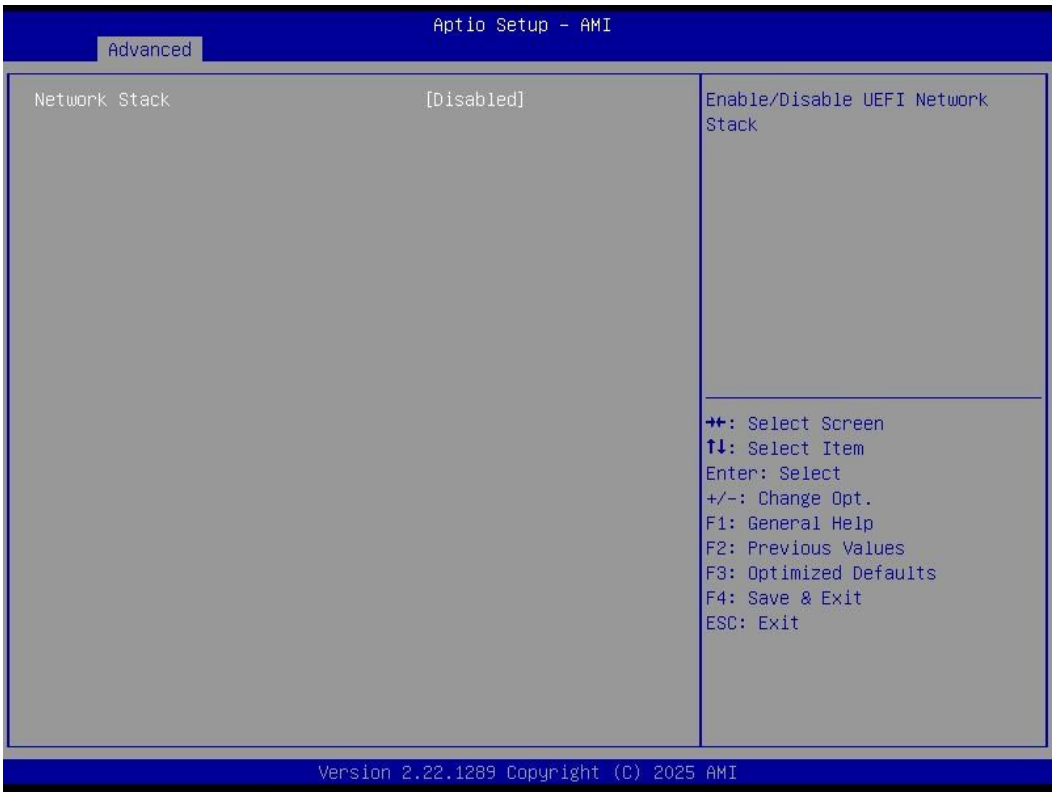


USB Devices
Displays all detected USB devices.

USB Mass Storage Driver Support
USB Mass Storage Driver support in BIOS, this feature allows USB storage enable or disable boot capability if USB storage can boot to DOS or UEFI shell.

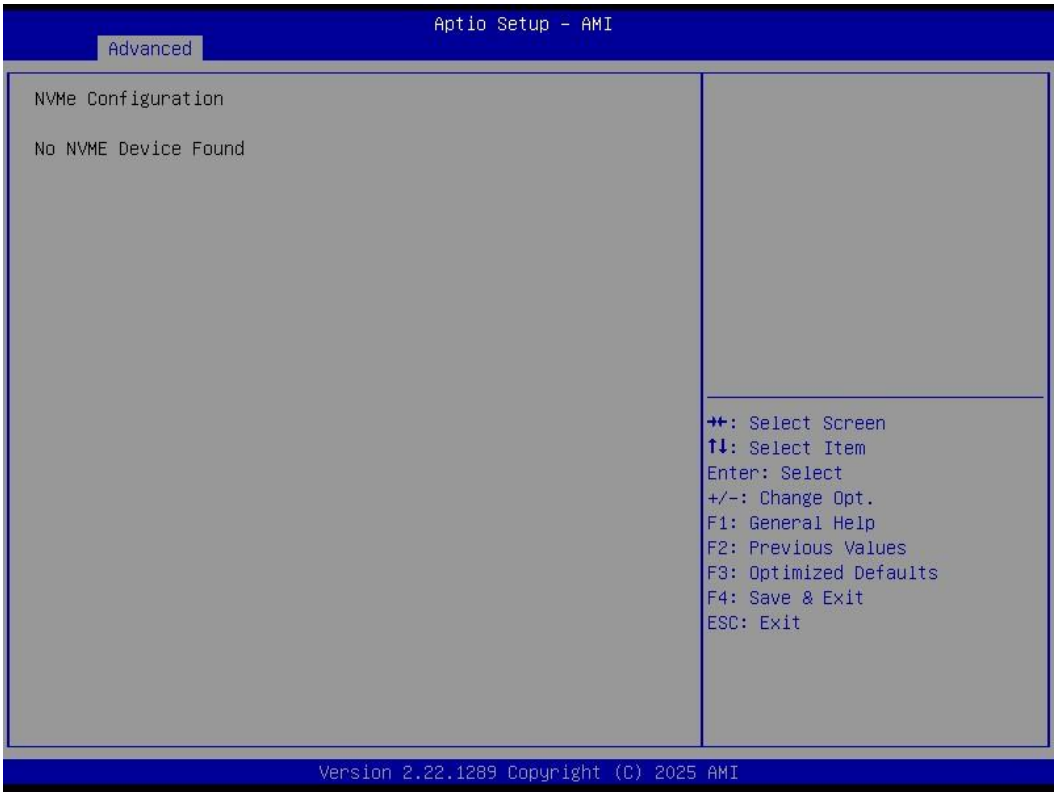
Mass Storage Devices
Mass storage device emulation type. Auto option enumerates devices according to their media format. Optical drives are emulated as CDROM, drives with no media will be emulated according to a drive type.

- **Network Stack Configuration**
  This screen provides function for specifying Network Stack Configuration.



Network Stack
Enable or disable Network stack function. When disabled, IPv4 PXE boot support will not be available.

- **NVMe Configuration**
  This screen displays the current NVMe configuration. Options are available only when a NVMe device is detected.

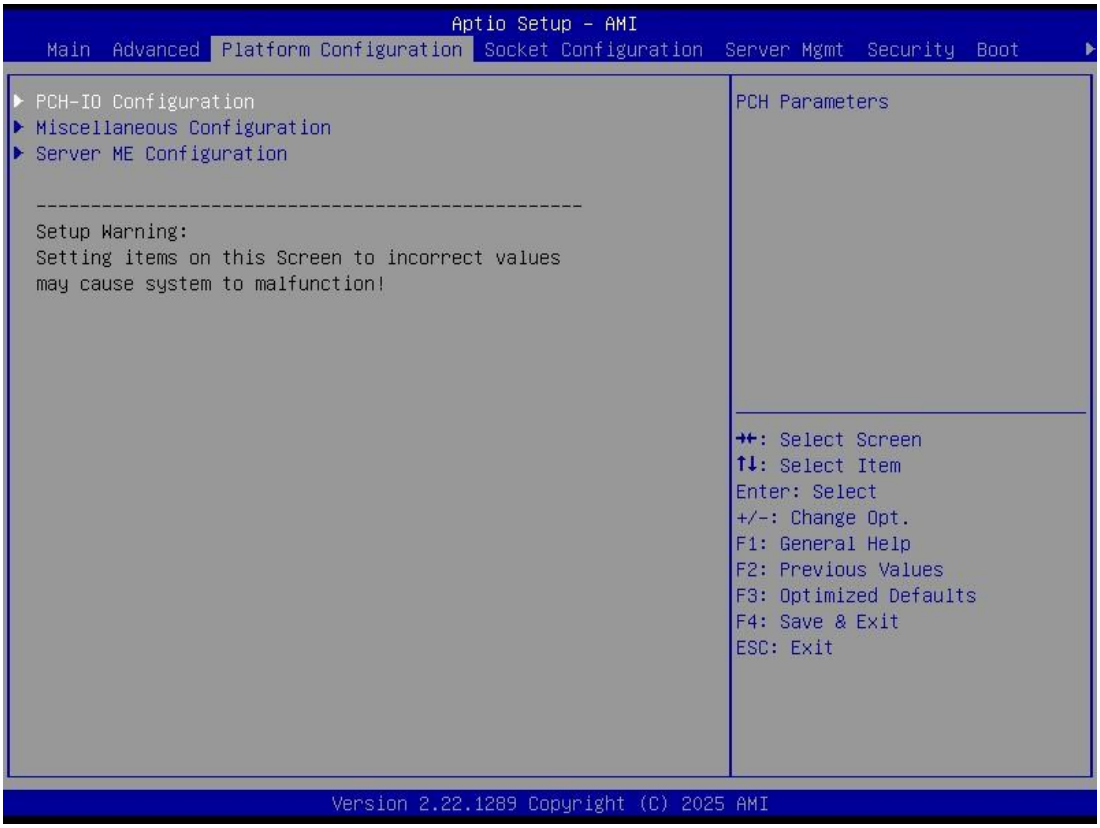


4.5 Platform Configuration

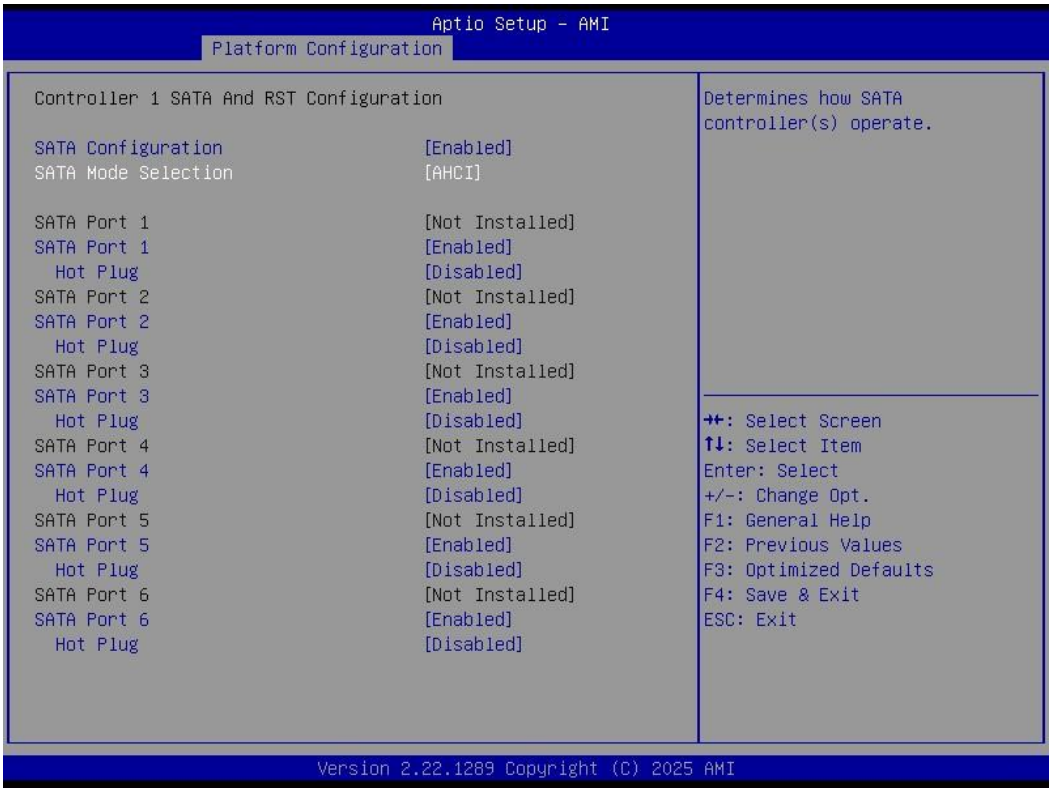
The platform configuration menu allows users to change the advanced platform configuration settings. You can select any of the items in the left frame of the screen to go to the sub menus:

- ► PCH-IO Configuration
- ► Miscellaneous Configuration
- ► Server ME Configuration

For items marked with "►", please press <Enter> for more options.



- **PCH-IO Configuration**
  The BIOS automatically detects any connected SATA devices during system boot up. The detected devices are displayed on this screen.



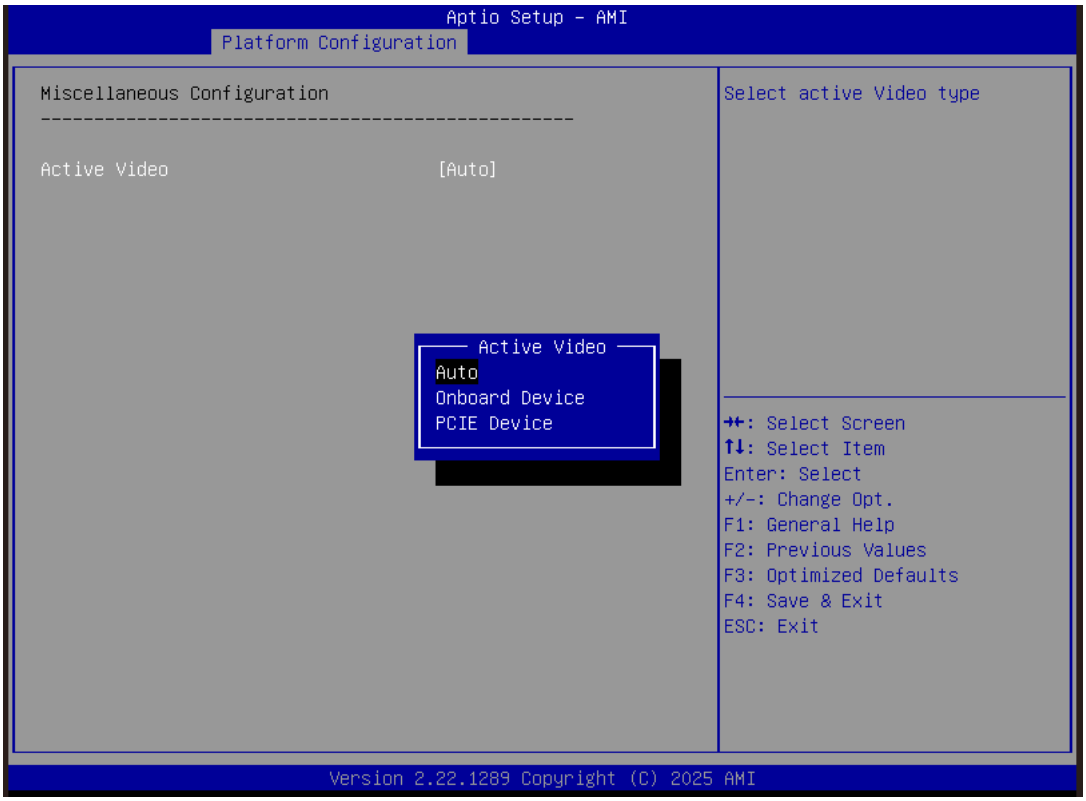
SATA Configuration
Enable or disable the SATA Controller feature. The default is Enabled.

SATA Mode Selection
Determine how SATA controller(s) operate. Options are RAID and AHCI (Advanced Host Controller Interface). The default is the AHCI mode.

SATA Port
Enable or disable the SATA port.

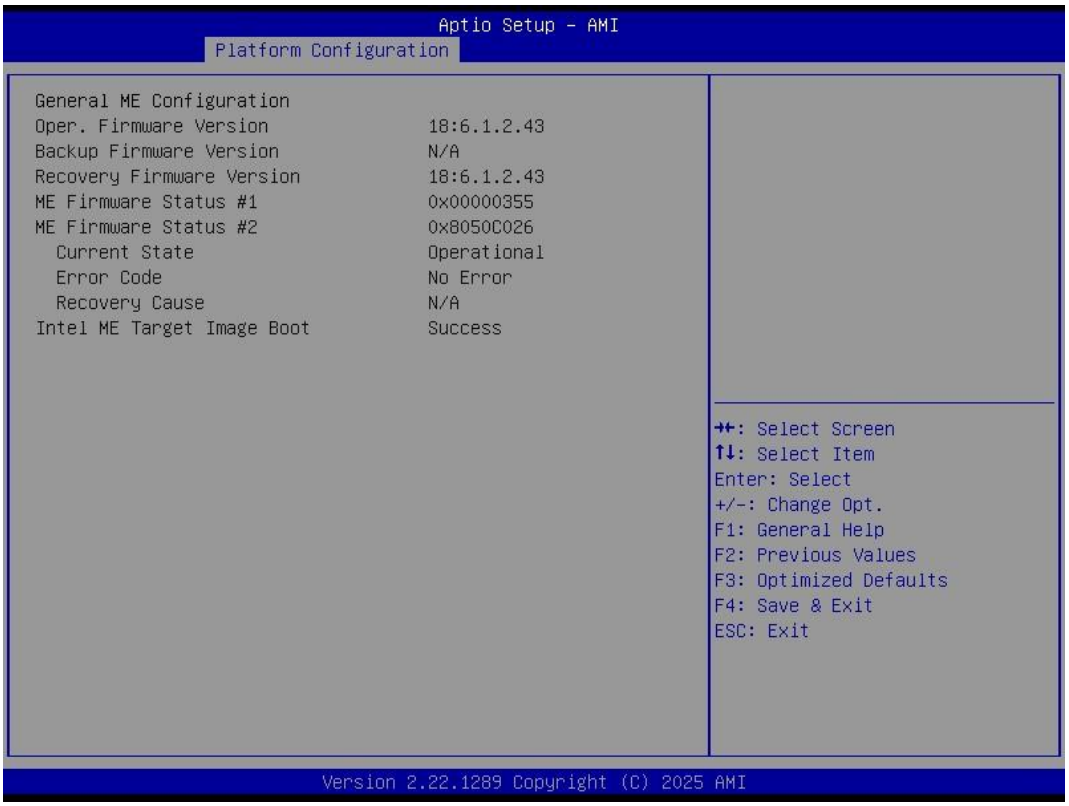
Hot Plug
Designates this port as Hot Pluggable.

- **Miscellaneous Configuration**
  Configure various other devices and functions.



Active Video
Set the display to auto-detect mode, specify an external PCIe graphics card, or specify the onboard graphics as the primary display.

- **Server ME Configuration**
  This screen displays ME configuration information.

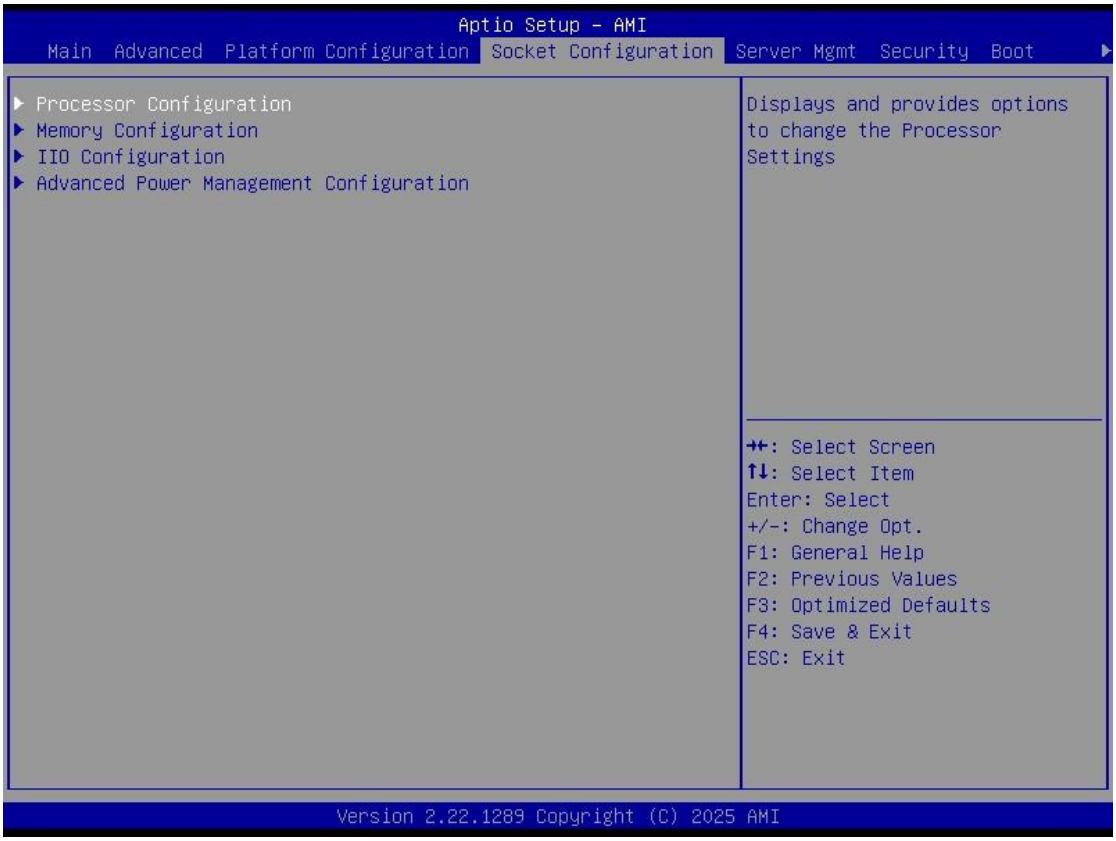


4.6 Socket Configuration

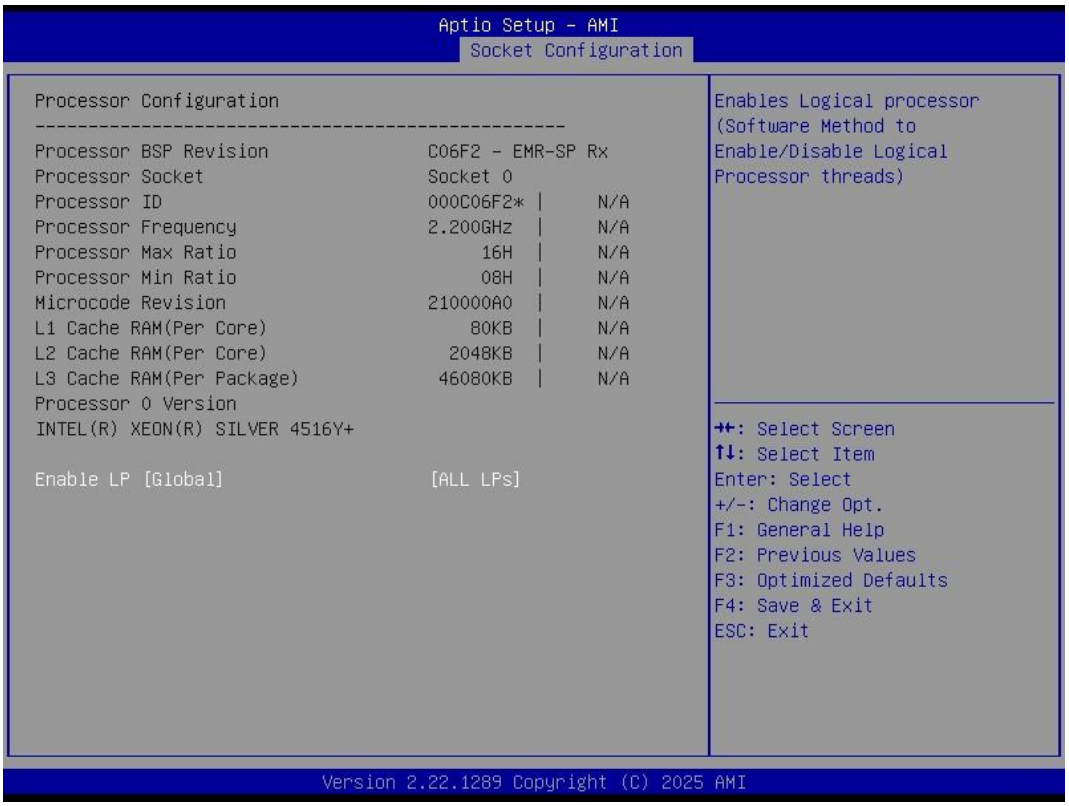
The socket configuration menu allows users to change the advanced socket settings.

- ► Processor Configuration
- ► Memory Configuration
- ► IIO Configuration
- ► Advanced Power Management Configuration

For items marked with "►", please press <Enter> for more options.

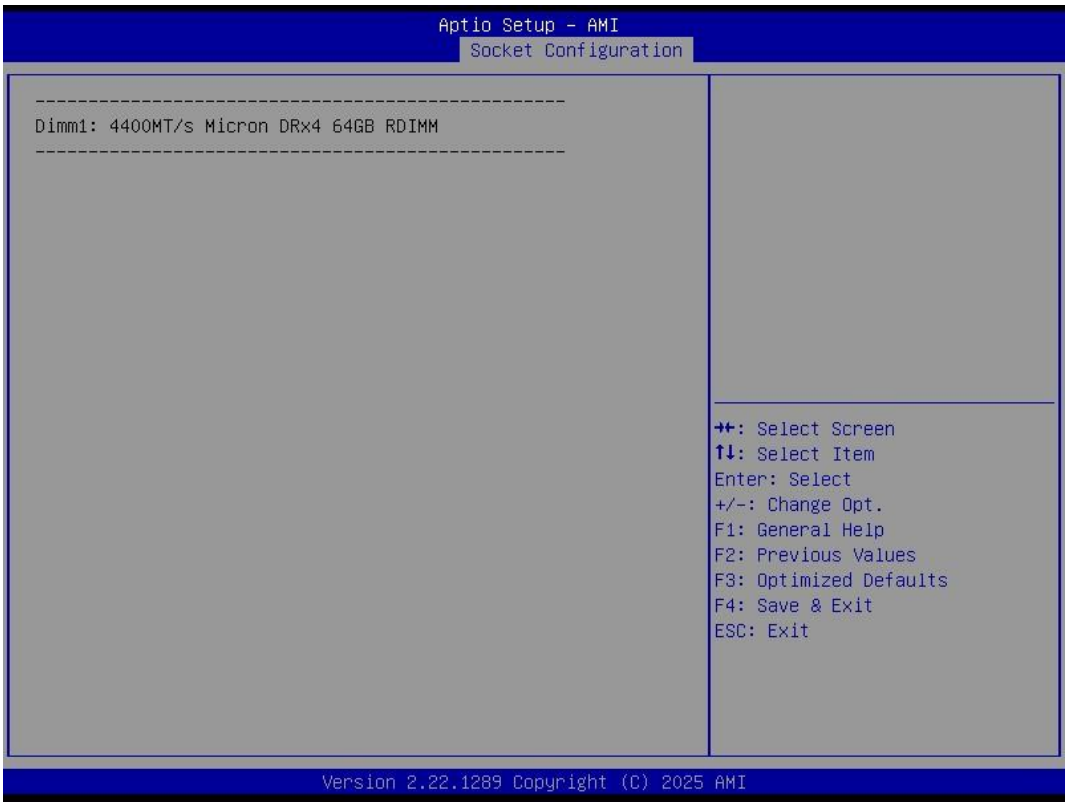


- **Processor Configuration**
  This screen shows processor information.

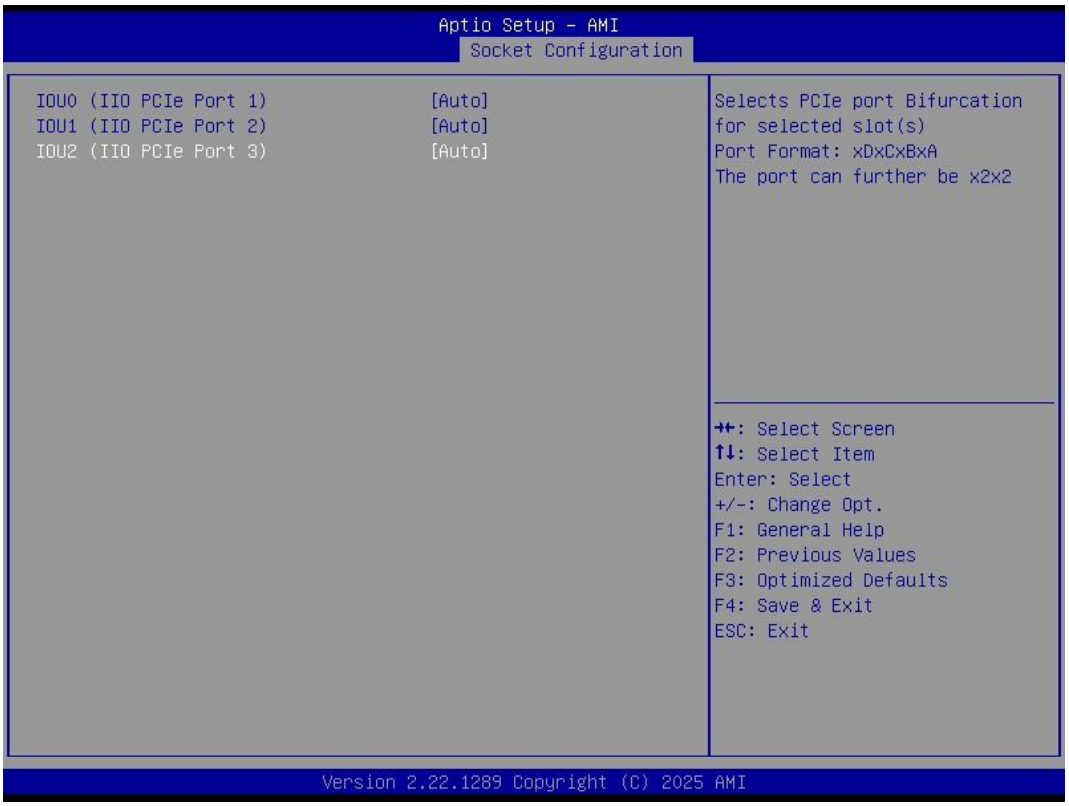


Enable LP [Global]
Enables Logical processor (Software Method to Enable/Disable Logical Processor threads).

- **Memory Configuration**
  This screen shows memory information.

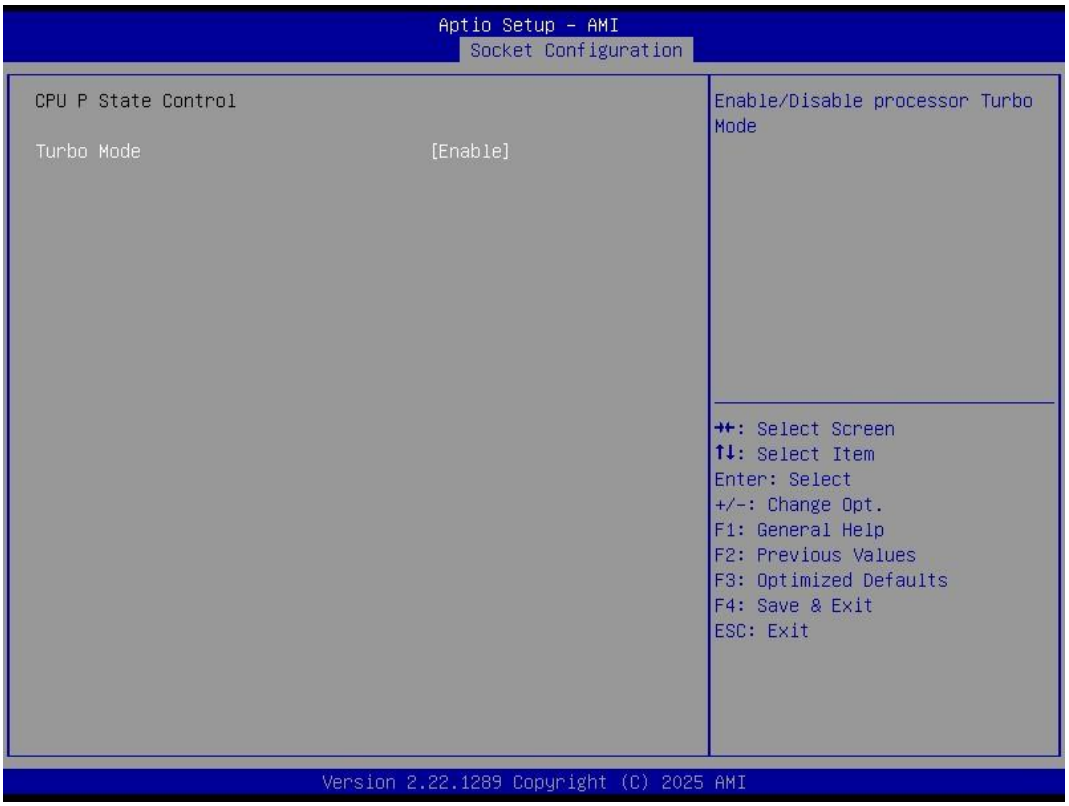


- **IIO Configuration**
  This screen shows the IO configuration information.



IOU0 / IOU1 / IOU2 (IIO PCIe Port 1~3)
Defines the PCIe bifurcation mode for the corresponding port. Port format: xCxBxA. The port can also be configured as x_x8_x8 or x_x_x_16 or Auto.

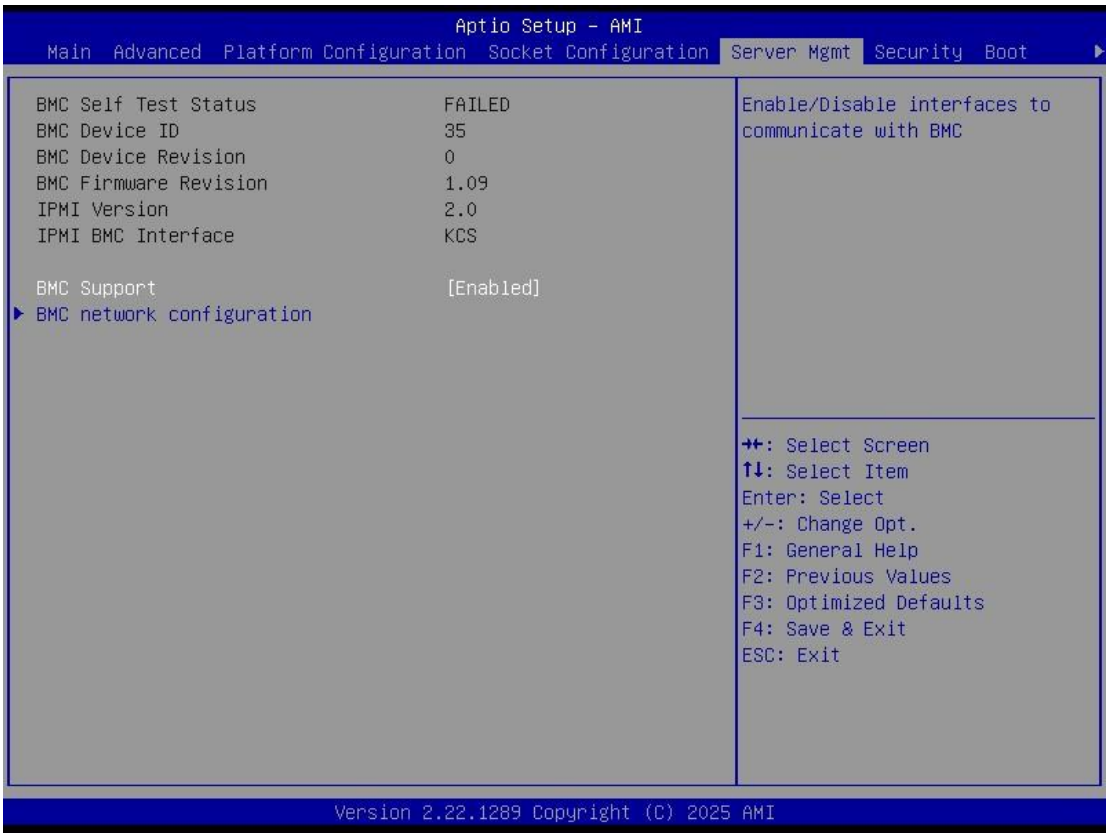
- **Advanced Power Management Configuration**
  This screen allow you to modify CPU power management and configure Turbo Mode.



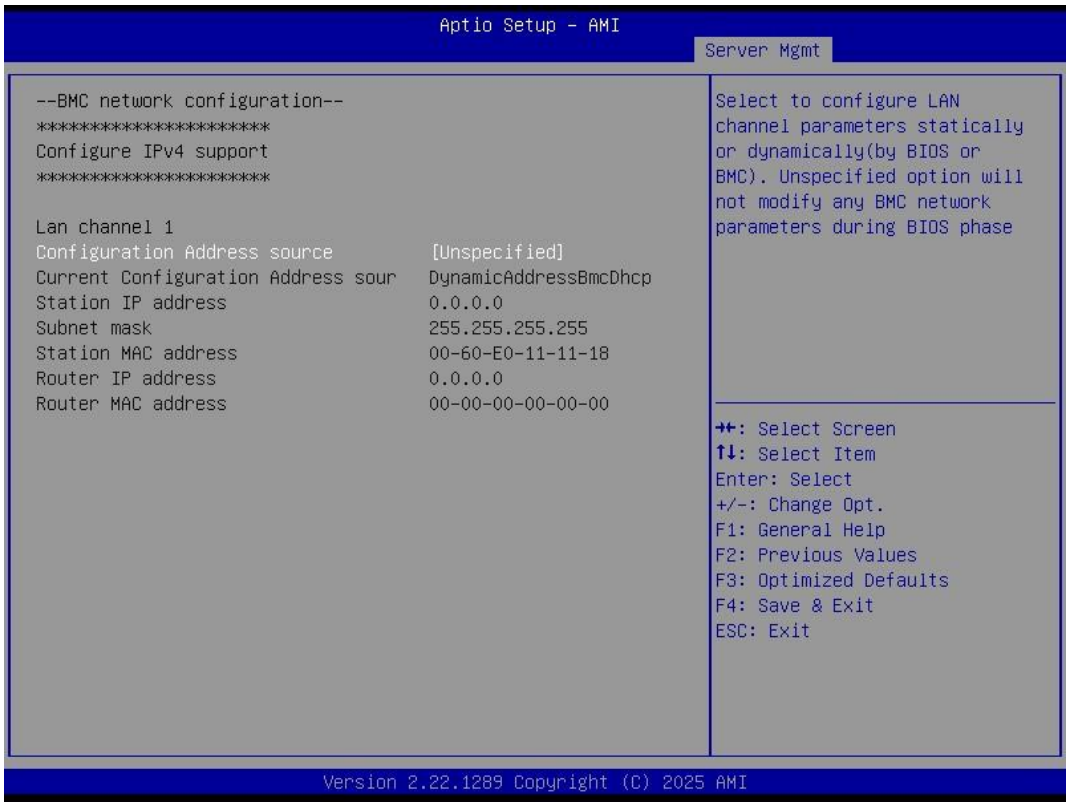
Turbo Mode
Enable/disable processor Turbo Mode. It allows processor cores to run faster but not exceed CPU defined frequency limits.

4.7 Server Management

The screen allows users to change the settings for the BMC.

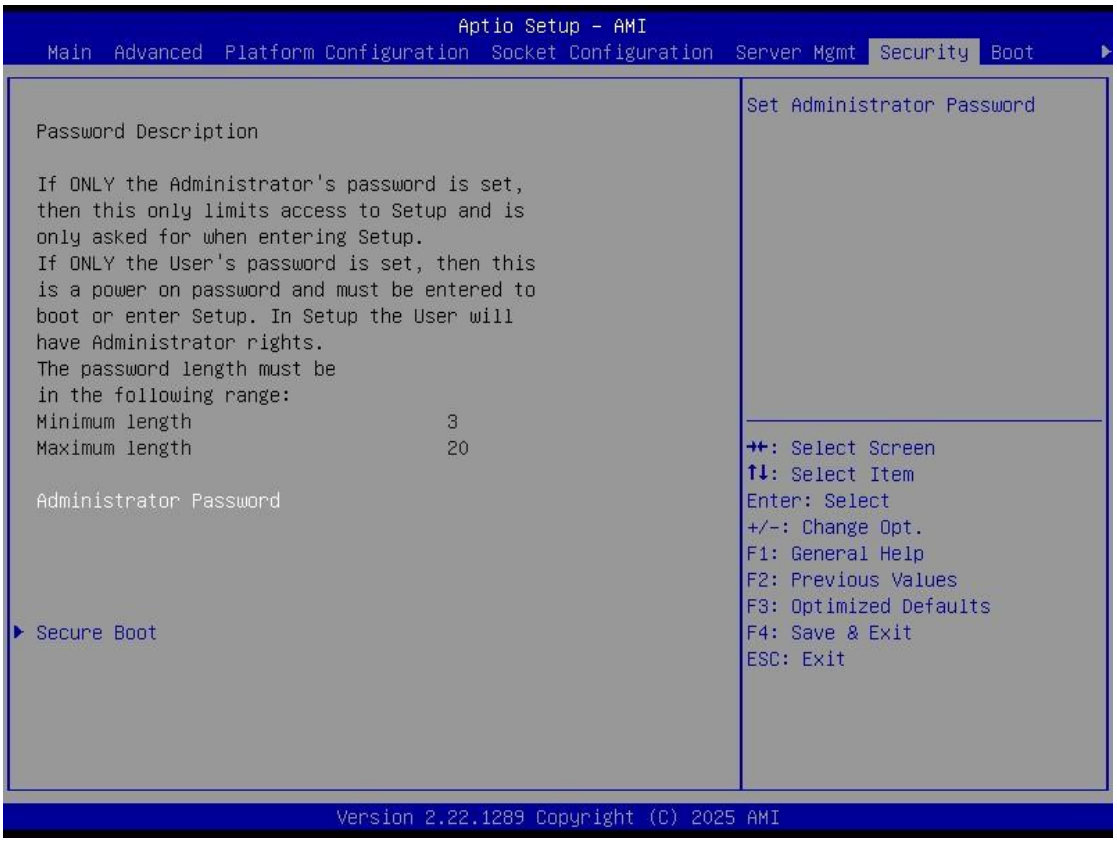


- **BMC Network Configuration**
  Select to configure LAN channel parameters statically or dynamically (by BMC).



4.8 Security Menu

The Security menu allows users to change the security settings for the system.

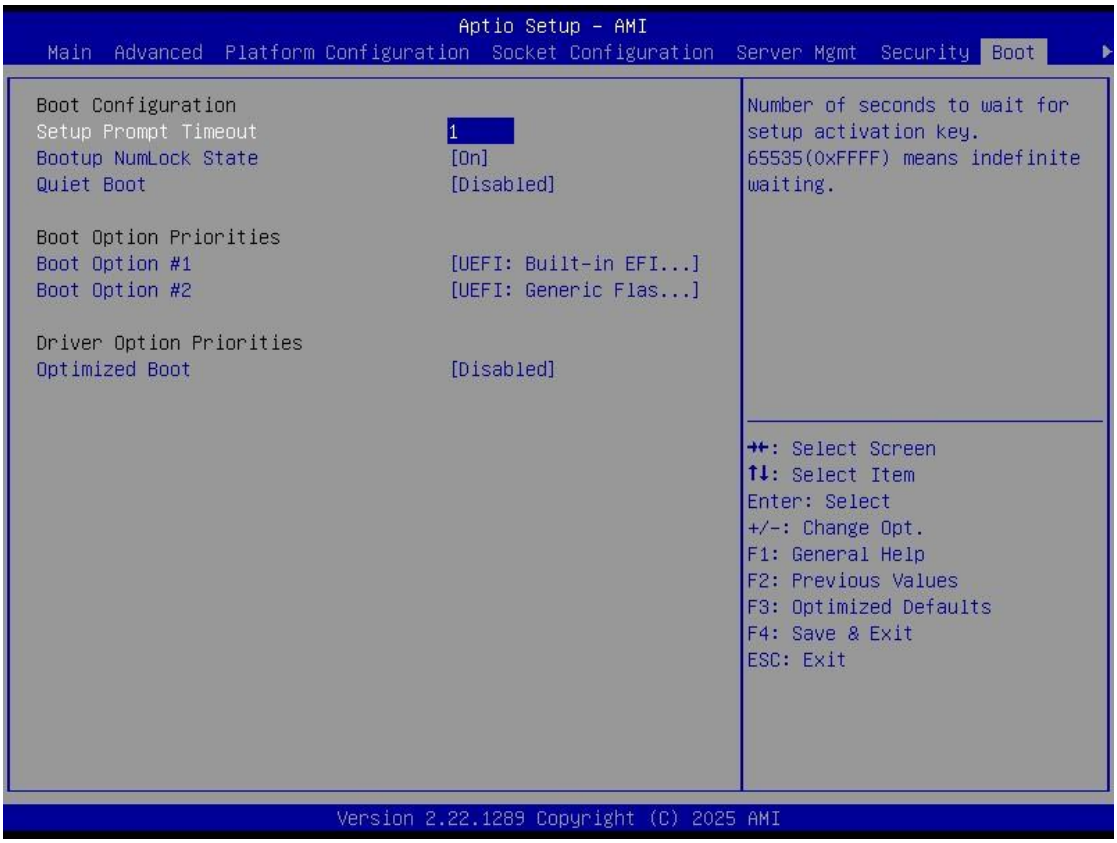


Administrator Password
This item indicates whether an administrator password has been set (installed or uninstalled).

Secure Boot
Use this item to set parameters related to Secure Boot.

4.9 Boot Menu

The Boot menu allows users to change boot options of the system.



Setup Prompt Timeout
Enter the number of seconds to wait for the setup activation key. 65535(0xFFFF) means indefinite waiting.

Bootup NumLock State
Use this item to select the power-on state for the keyboard NumLock.

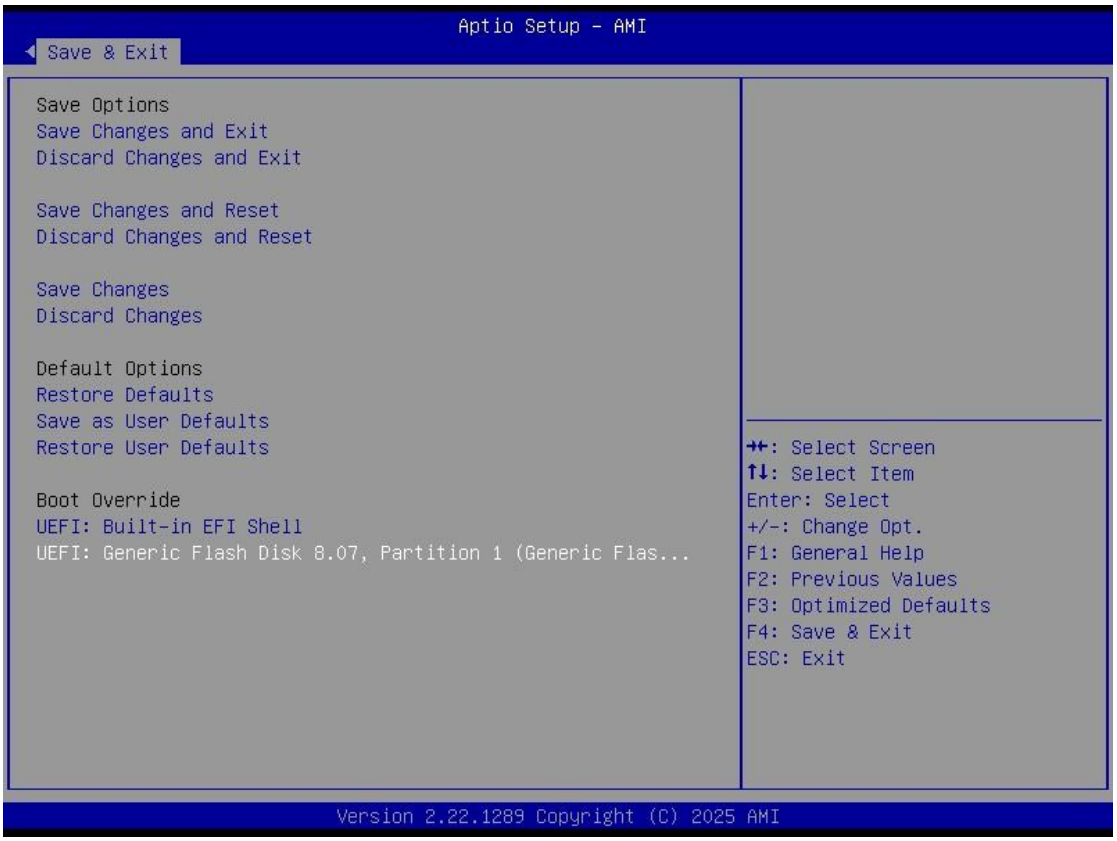
Quiet Boot
Select to display either POST output messages or a splash screen during boot-up.

Boot Option Priorities [Boot Option #1, …]
These are settings for boot priority. Specify the boot device priority sequence from the available devices.

Optimized Boot
Use this function when the system BIOS boots with native UEFI graphics drivers. It allows you to enable Optimized Boot for compatibility with VMware ESXi on systems configured for UEFI Boot Mode, and to enable Secure Boot Mode.

4.10 Save & Exit Menu

The Save & Exit menu allows users to load your system configuration with optimal or fail-safe default values.



Save Changes and Exit
When you have completed the system configuration changes, select this option to leave Setup and return to Main Menu. Select Save Changes and Exit from the Save & Exit menu and press <Enter>. Select Yes to save changes and exit.

Discard Changes and Exit
Select this option to quit Setup without making any permanent changes to the system configuration and return to Main Menu. Select Discard Changes and Exit from the Save & Exit menu and press <Enter>. Select Yes to discard changes and exit.

Save Changes and Reset
When you have completed the system configuration changes, select this option to leave Setup and reboot the computer so the new system configuration parameters can take effect. Select Save Changes and Reset from the Save & Exit menu and press <Enter>. Select Yes to save changes and reset.

Discard Changes and Reset
Select this option to quit Setup without making any permanent changes to the system configuration and reboot the computer. Select Discard Changes and Reset from the Save & Exit menu and press <Enter>. Select Yes to discard changes and reset.

Save Changes
When you have completed the system configuration changes, select this option to save changes. Select Save Changes from the Save & Exit menu and press <Enter>. Select Yes to save changes.

Discard Changes
Select this option to quit Setup without making any permanent changes to the system configuration. Select Discard Changes from the Save & Exit menu and press <Enter>. Select Yes to discard changes.

Restore Defaults
It automatically sets all Setup options to a complete set of default settings when you select this option. Select Restore Defaults from the Save & Exit menu and press <Enter>.

Save as User Defaults
Select this option to save system configuration changes done so far as User Defaults. Select Save as User Defaults from the Save & Exit menu and press <Enter>.

Restore User Defaults
It automatically sets all Setup options to a complete set of User Defaults when you select this option. Select Restore User Defaults from the Save & Exit menu and press <Enter>.

Boot Override
Select a drive to immediately boot that device regardless of the current boot order.

This page is intentionally left blank.

Appendix A
Watchdog Timer

About Watchdog Timer

Software stability is a major issue in most applications. Some embedded systems are not watched by humans for 24 hours. It is usually too slow to wait for someone to reboot when computer hangs. The systems need to be able to reset automatically when things go wrong. The watchdog timer gives us that solution.

The watchdog timer is a counter that triggers a system reset when it counts down to zero from a preset value. The software starts the counter with an initial value and must reset it periodically. If the counter ever reaches zero which means the software has crashed, the system will reboot.

How to Use Watchdog Timer

```
//////////////////////////////////////////////////////////////////////
////////////////////
#include <stdio.h>
#include <stdlib.h>

#include <sys/io.h>

#define SIO_INDEX 0x4E
#define SIO_DATA  0x4F

#define SIO_ENTRY_KEY  0x87
#define SIO_EXIT_KEY   0xAA

#define SIO_LD_WDT  0x07

#define SIO_REG_LDN         0x07
#define SIO_REG_ACTIVATE    0x30
#define SIO_REG_IOBASE_HIGH  0x60
#define SIO_REG_IOBASE_LOW   0x61

#define WDT_IOBASE_HIGH 0x02
#define WDT_IOBASE_LOW 0x50
#define WDT_IOBASE 0x0250
#define WDT_CONFIG 0x05
#define WDT_TIME   0x06


int main()
{
  unsigned char Count = 10; // 10 Seconds
  unsigned char DataBuffer; // Operate Io Data

  //Get  Io Port Read/Write Permission
  iopl(3);

  //Enter SIO Config
  outb_p ( SIO_ENTRY_KEY, SIO_INDEX);
```

```
  outb_p ( SIO_ENTRY_KEY, SIO_INDEX);


  // Set WDT IOBASE
  // Select Logical Device = 07 (WDT)
  outb_p ( SIO_REG_LDN , SIO_INDEX);
  outb_p ( SIO_LD_WDT  , SIO_DATA);

  // set IOBase
  outb_p ( SIO_REG_IOBASE_HIGH , SIO_INDEX);
  outb_p ( WDT_IOBASE_HIGH ,    SIO_DATA);

  outb_p ( SIO_REG_IOBASE_LOW , SIO_INDEX);
  outb_p ( WDT_IOBASE_LOW ,    SIO_DATA);

  // Activate Wdt IO Decode
  outb_p ( SIO_REG_ACTIVATE , SIO_INDEX);
  outb_p ( 1              , SIO_DATA);

  //Exit SIO Config
  outb_p ( SIO_EXIT_KEY, SIO_INDEX);


  // Clear And Set Wdt Status
  /*
  Wdt Config Reg Bit Definition
  7 : Reserved
  6 : WDT time out Status (Write 1 Clear)
  5 : Watch dog counting Enable
  4 : Set Output mode (0 Level,1 Edge)
  3 : Time Unit (0 : 1sec , 1: 60Sec)
  2 : Output Polarity (0 : low active , 1 : High active)
  1-0 : (output pulse width of Wdtrst# ,
        00 1ms  , 01 25ms ,
       10 125ms ,11 :5sec)
  */
  outb_p ( 0x40  ,  WDT_IOBASE + WDT_CONFIG);

  //Set WatchDog Count Time
  outb_p ( Count ,  WDT_IOBASE + WDT_TIME);

  //Start WatchDog Count
  outb_p ( 0x20  ,  WDT_IOBASE + WDT_CONFIG);

  //Print Remain Time
  while(1)
  {
    DataBuffer = inb_p ( WDT_IOBASE + WDT_TIME );
    printf(" reset in %d sec\n",DataBuffer);
  }
  return 0;
}
//////////////////////////////////////////////////////////////////////
//////////////////////
```

Appendix B
Configuring SATA for RAID

Configuring SATA Hard Drive(s) for RAID Function

Before you begin the SATA configuration, please prepare:

- Two SATA hard drives (to ensure optimal performance, it is recommended that you use two hard drives with identical model and capacity). If you do not want to create RAID with the SATA controller, you may prepare only one hard drive.

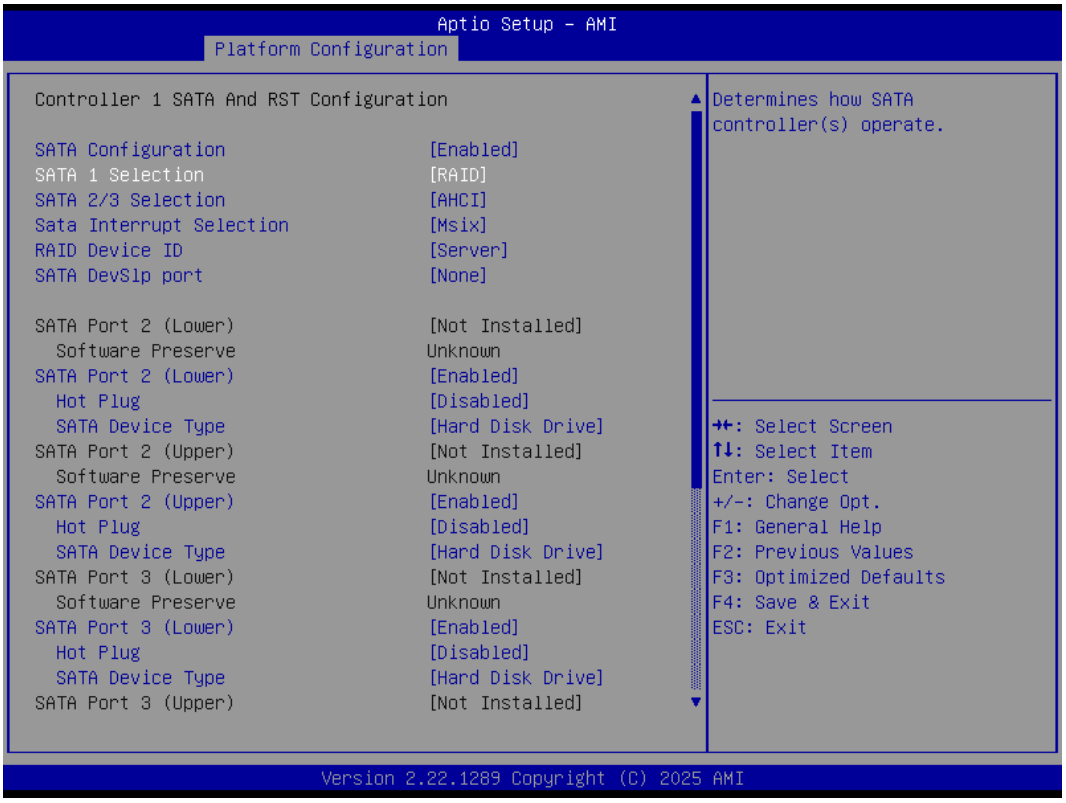
Please follow up the steps below to configure SATA hard drive(s):

1. Install SATA hard drive(s) in your system.
2. Enter the BIOS Setup to configure SATA controller mode and boot sequence.
3. Configure RAID by the RAID BIOS.

1. Installing SATA hard drive(s) in your system.
Connect one end of the SATA signal cable to the rear of the SATA hard drive, and the other end to available SATA port(s) on the board. Then, connect the power connector of power supply to the hard drive.

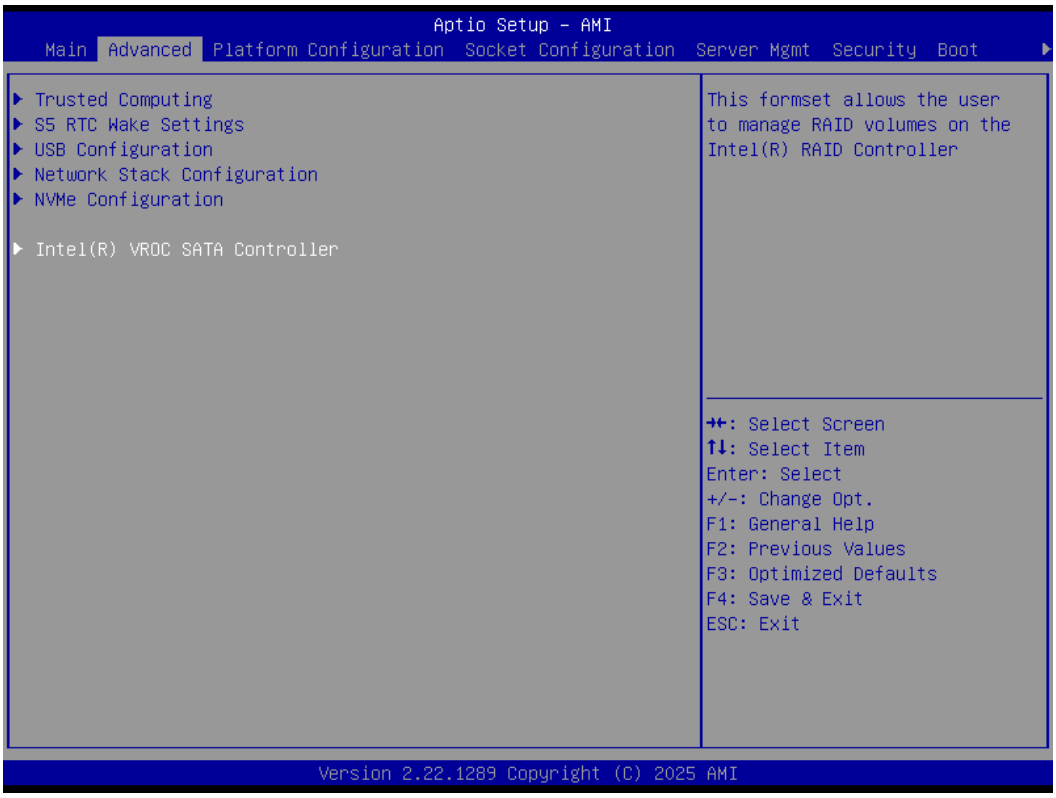
2. Configuring SATA controller mode and boot sequence by the BIOS Setup.
You have to make sure whether the SATA controller is configured correctly by system BIOS Setup and set up BIOS boot sequence for the SATA hard drive(s).

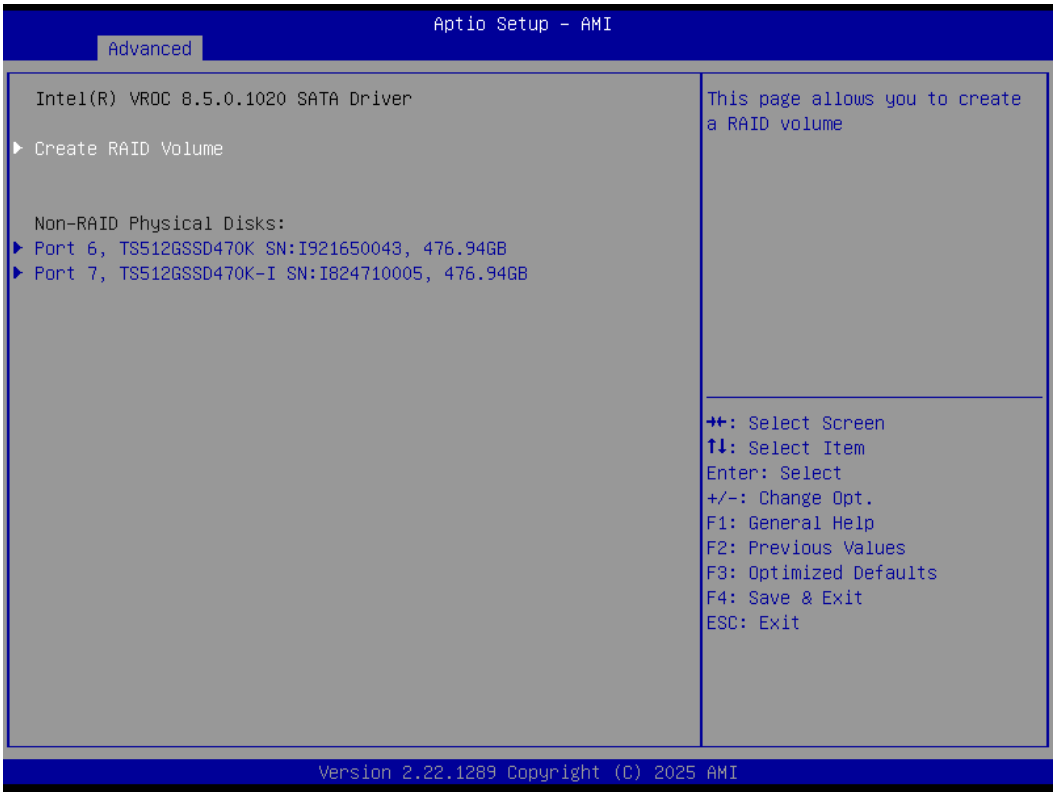
2.1. Turn on your system, and then press the <Del> button to enter BIOS Setup during running POST (Power-On Self Test). If you want to create RAID, just go to the Platform configuration/PCH SATA Configuration, select the “Configuration SATA as”, and press <Enter> for more options. A list of options appears, please select “RAID”.



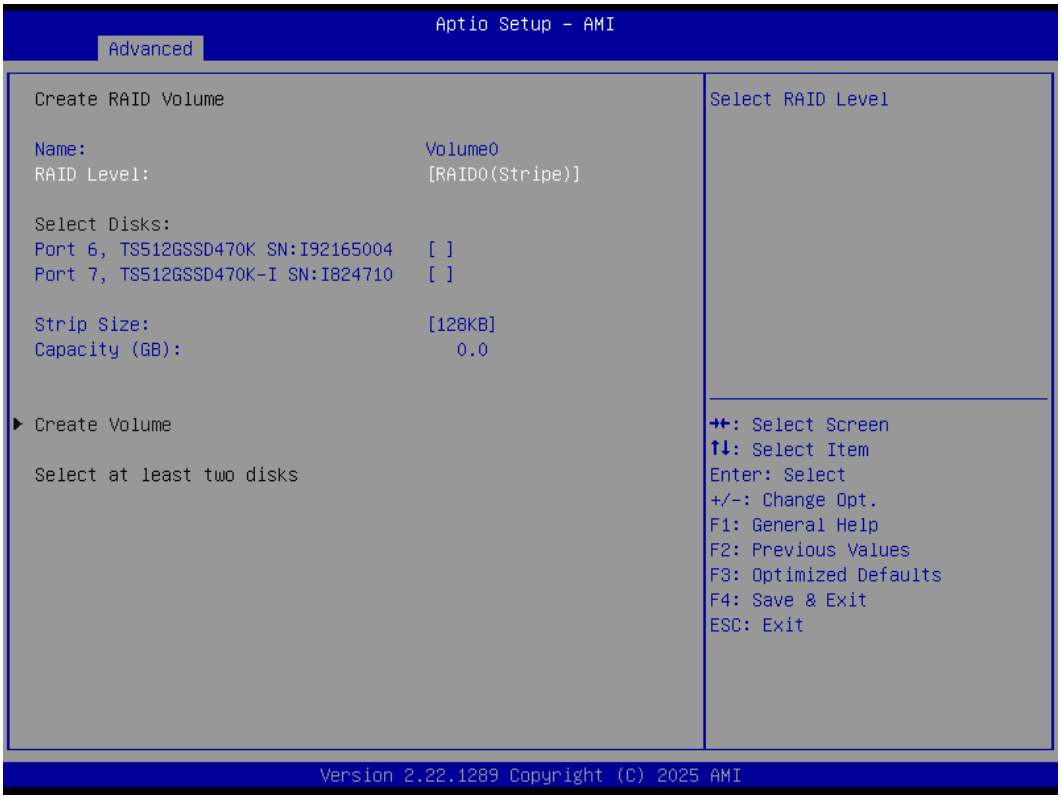
2.2. Save and exit the BIOS Setup.

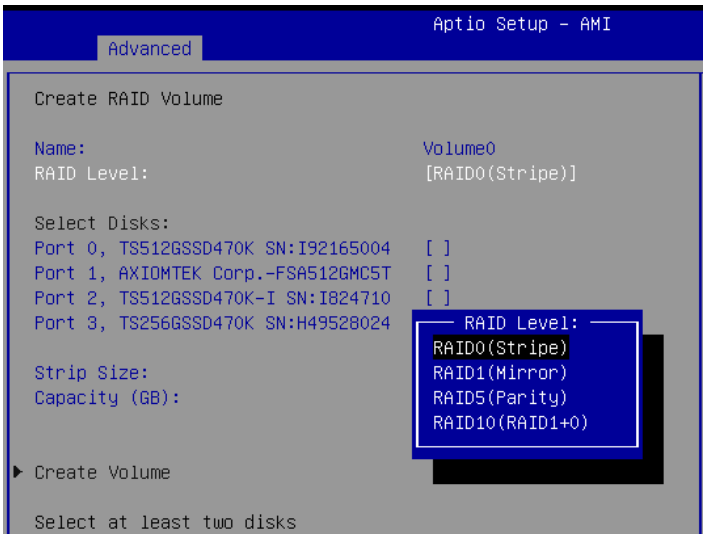
2.3. Go to the Advanced screen, select the “Intel(R) VROC SATA Controller”; furtherly, select the ”Create RAID Volume” and press <Enter> for more options.





2.4. Select the “RAID Level”, and choose RAID0, 1, 5 or 10 based on your needs.





2.5. Save and exit the BIOS Setup.

Appendix C
Digital I/O

Digital I/O Software Programming

- SMBUS to GPIO PCA9554PW GPIO[3:0] is Output, GPIO[7:4] is Input.
- SMBUS Slave address: 0x44.
- IOBASE: 0x3000
- Registers:

Command byte

Command	Protocol	Function
0	Read byte	Input port register
1	Read/write byte	Output port register
2	Read/write byte	Polarity inversion register
3	Read/write byte	Configuration register

The command byte is the first byte to follow the address byte during a write transmission. It is used as a pointer to determine which of the following registers will be written or read.

Register 0: Input port register.
This register is a read-only port. It reflects the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output by Register 3. Writes to this register have no effect.

The default 'X' is determined by the externally applied logic level, normally '1' when no external signal is externally applied because of the internal pull-up resistors.

Bit	Symbol	Access	Value	Description
7	I7	Read only	X	Determined by externally applied logic level.
6	I6	Read only	X	
5	I5	Read only	X	
4	I4	Read only	X	
3	I3	Read only	X	
2	I2	Read only	X	
1	I1	Read only	X	
0	I0	Read only	X	

Register 1: Output port register.
This register reflects the outgoing logic levels of the pins defined as outputs by Register 3. Bit values in this register have no effect on pins defined as inputs. Reads from this register return the value that is in the flip-flop controlling the output selection, not the actual pin value.

Bit	Symbol	Access	Value	Description
7	O7	R	1*	Reflects outgoing logic levels of pins defined as outputs by Register 3.
6	O6	R	1*	
5	O5	R	1*	
4	O4	R	1*	
3	O3	R	1*	
2	O2	R	1*	
1	O1	R	1*	
0	O0	R	1*	

* : Default value

Register 2: Configuration register.
This register configures the directions of the I/O pins. If a bit in this register is set, the corresponding port pin is enabled as an input with high-impedance output driver. If a bit in this register is cleared, the corresponding port pin is enabled as an output. At reset, the I/Os are configured as inputs with a weak pull-up to VDD.

Bit	Symbol	Access	Value	Description
7	C7	R/W	1*	Configure the directions of the I/O pins. 0 = Corresponding port pin enabled as an output. 1 = Corresponding port pin configured as input (default value).
6	C6	R/W	1*	
5	C5	R/W	1*	
4	C4	R/W	1*	
3	C3	R/W	1*	
2	C2	R/W	1*	
1	C1	R/W	1*	
0	C0	R/W	1*	

* : Default value

Sample Code

```
//////////////////////////////////////////////////////////////////////
#include <stdio.h>
#include <stdlib.h>

#include <sys/io.h>

//SMBUS IO base, Host Status Register Address(HSTS)
#define HSTS 0x3000
//Host Control Register (HCTL)
#define HCTL 0x3002
//Host Command Register (HCMD)
#define HCMD 0x3003
//Transmit Slave Address Register (TSA)
#define TSA 0x3004
//Data 0 Register (HD0)
#define HD0 0x3005
#define DIO_SLAVE_ADDR_WRITE 0x44
#define DIO_SLAVE_ADDR_READ 0x45
#define DIO_INPUT_OFFSET 0x00
#define DIO_OUTPUT_OFFSET 0x01
#define DIO_CONFIG_OFFSET 0x03

// Set DIO to output and print configuration register value
int SetDIO_to_output()
{
  unsigned char config_value;
  //Get Io Port Read/Write Permission
  iopl(3);
  // Clear host status register
  outb_p (0xFF, HSTS);

  //Set DIO device slave address and set command to write(slave //addr+0)
  outb_p ( DIO_SLAVE_ADDR_WRITE, TSA);

  //Set DIO offset to configuration register
  outb_p ( DIO_CONFIG_OFFSET, HCTL);

  //Set DIO configuration register bit 0~7 to 0 which means set all
  //DIO ports to output (0 -> output, 1 -> input)
  outb_p (0x0, HD0);

  //Raise the START bit(bit 6) of HCTL and set SMB_CMD (bit2~4) of
  //HCTL to 0x010(Byte Data) to start transfer
  outb_p (0x48, HCTL);

  //print configuration register value
  // Clear host status register
  outb_p (0xFF, HSTS);

  //Set DIO device slave address and set command to read(slave //addr+1)
  outb_p ( DIO_SLAVE_ADDR_READ, TSA);

  //Set DIO offset to configuration register
  outb_p ( DIO_CONFIG_OFFSET, HCTL);

  //Raise the START bit(bit 6) of HCTL and set SMB_CMD (bit2~4) of
  //HCTL to 0x010(Byte Data) to start transfer
```

```
  outb_p (0x48, HCTL);
  //Read from HS0 to print configuration register value
  config_value = inb_p (HD0);
  printf(" configuration value = %d\n",config_value);

  return 0;
}

// Set DIO output to low/high
int SetDIOoutput_low_high()
{
  //Get Io Port Read/Write Permission
  iopl(3);
  // Clear host status register
  outb_p (0xFF, HSTS);

  //Set DIO device slave address and set command to write(slave //addr+0)
  outb_p ( DIO_SLAVE_ADDR_WRITE, TSA);

  //Set DIO offset to output register
  outb_p ( DIO_OUTPUT_OFFSET, HCTL);

  //Set DIO 0~3 output low, 4~7 output high by configure DIO output
  //port register bit 0~7, 0x0F means bit 0~3 =1, 4~7 =0, 0-> low,
  // 1->high
  outb_p (0x0F, HD0);
  //Raise the START bit(bit 6) of HCTL and set SMB_CMD (bit2~4) of
  //HCTL to 0x010(Byte Data) to start transfer
  outb_p (0x48, HCTL);

  return 0;
}

// Set DIO to input and print status (should be 0xFF, all ports read
high)
int SetDIO_to_input()
{
  unsigned char input_value;
  //Get Io Port Read/Write Permission
  iopl(3);
  // Clear host status register
  outb_p (0xFF, HSTS);

  //Set DIO device slave address and set command to write(slave //addr+0)
  outb_p ( DIO_SLAVE_ADDR_WRITE, TSA);

  //Set DIO offset to configuration register
  outb_p ( DIO_CONFIG_OFFSET, HCTL);

   //Set DIO configuration register bit 0~7 to 1 which means set all
   //DIO ports to input (0 -> output, 1 -> input)
  outb_p (0xFF, HD0);

  //Raise the START bit(bit 6) of HCTL and set SMB_CMD (bit2~4) of
  //HCTL to 0x010(Byte Data) to start transfer
  outb_p (0x48, HCTL);

  //print configuration register value
  // Clear host status register
  outb_p (0xFF, HSTS);
```

```
  //Set DIO device slave address and set command to read(slave //addr+1)
  outb_p ( DIO_SLAVE_ADDR_READ, TSA);

  //Set DIO offset to configuration register
  outb_p ( DIO_INPUT_OFFSET, HCTL);

  //Raise the START bit(bit 6) of HCTL and set SMB_CMD (bit2~4) of
  //HCTL to 0x010(Byte Data) to start transfer
  outb_p (0x48, HCTL);
  //Read from HS0 to print configuration register value
  input_value = inb_p (HD0);
  printf(" input value = %d\n",input_value);

  return 0;
}
```