USER'S MANUAL

CAPA561

LGA1700 socket for 13th/ 12th Generation Intel® Core™ Processor Family 3.5" Board

User's Manual

AXIOMTEK

www.axiomtek.com

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CAUTION

If you replace wrong batteries, it causes the danger of explosion. It is recommended by the manufacturer that you follow the manufacturer's instructions to only replace the same or equivalent type of battery, and dispose of used ones.

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ESD Precautions

Computer boards have integrated circuits sensitive to static electricity. To prevent chipsets from electrostatic discharge damage, please take care of the following jobs with precautions:

- Do not remove boards or integrated circuits from their anti-static packaging until you are ready to install them.
- Before holding the board or integrated circuit, touch an unpainted portion of the system unit chassis for a few seconds. It discharges static electricity from your body.
- Wear a wrist-grounding strap, available from most electronic component stores, when handling boards and components.

Trademarks Acknowledgments

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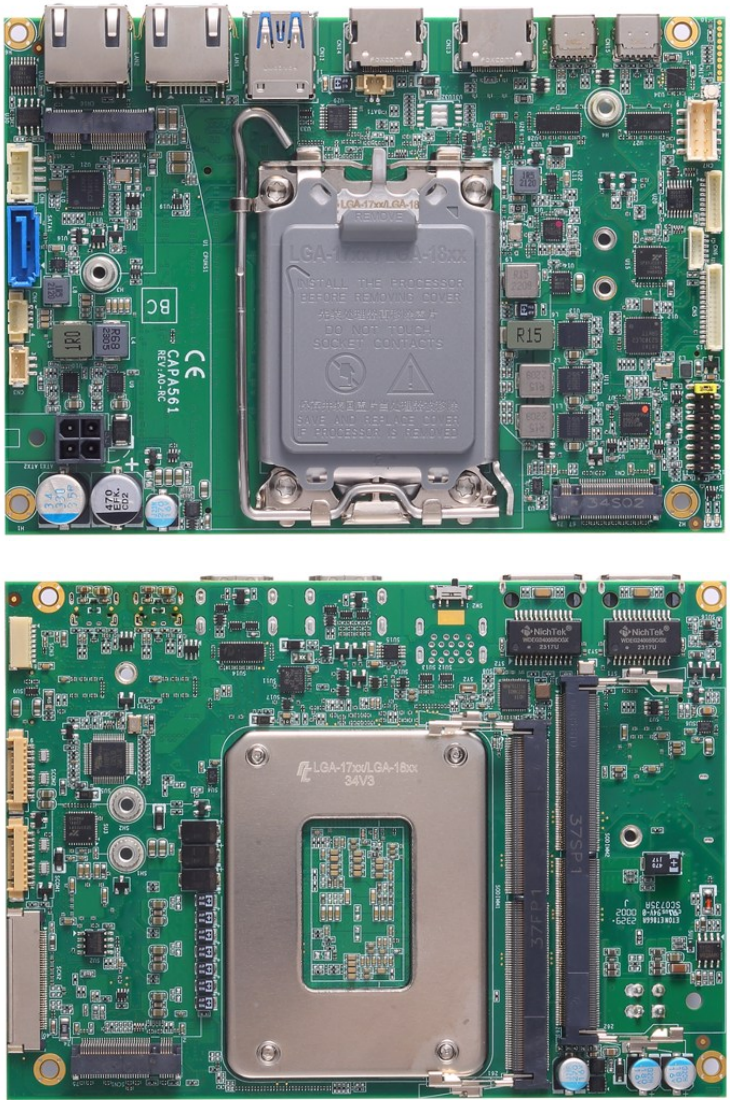
Section 1
Introduction



The CAPA561, a high performance 3.5" board, supports LGA1700 socket for 13th/ 12th Generation Intel® Core™ i7/ i5/ i3 processors. The board delivers outstanding system performance through high-bandwidth interfaces, multiple I/O functions for interactive applications and various embedded computing solutions.

There are two 262-pin unbuffered SO-DIMM socket for single channel DDR5 4800MHz memory supporting up to 64GB memory capacity. It also features three Ethernet ports (1 GbE and two 2.5 GbE), one SATA port with transfer rate up to 6Gb/s, two USB 3.2 in Type A, two USB 3.2 in Type C with DP Alt mode supported, also two USB 2.0 high speed compliant that can achieve the best stability and reliability for industrial applications. Additionally, it provides you with unique embedded features, such as two serial port (RS-232/422/485) and 3.5" form factor that applies an extensive array of PC peripherals.

1.1 Features

- LGA1700 socket for 13th/ 12th Generation Intel® Core™ i7/ i5/ i3/ Celeron®
- 2 DDR5 SO-DIMM supports up to 64GB memory capacity
- 2 USB 3.2 in Type A, 2 USB 3.2 in Type C with DP Alt mode supported and 2 USB 2.0 ports
- 2 COM port with RS232/422/485 supported
- 1 GbE LAN and 2 2.5GbE LAN
- 3 M.2 expansion slots

1.2 Specifications

- **CPU**
  - LGA1700 Socket

  Suggested CPU
  13th Gen
  - Intel® Core™ 7-150UL 10 core
  - Intel® Core™ 5-120UL 10 core
  - Intel® Core™ 3-100UL 6 core
  - Intel® processor U300L 5 core

  12th Gen
  - Intel® Core™ i7-1255UL 10 core
  - Intel® Core™ i5-1235UL 10 core
  - Intel® Celeron® processor 7305L 5 core

SpeedStep might be functioned to minimize power draw and heat generation.

Note

- **Chipset**
  - N/A

- **Thermal Solution and Operating Temperature**
  - Active: -20°C~70°C
  - Passive: -20°C~60°C

- **BIOS**
  - American Megatrends Inc. UEFI (Unified Extensible Firmware Interface) BIOS
  - 512Mbit SPI Flash, DMI, Plug and Play
  - PXE Ethernet Boot ROM

- **System Memory**
  - Two 262-pin unbuffered DDR5 SO-DIMM socket
  - Maximum up to 64GB DDR5 4800MHz memory capacity

- **Onboard Multi I/O**
  - Controller: Fintek F81804U
  - Serial Port: Two ports for RS-232/422/485.

- **Storage**
  - One SATA-600 connector
  - One M.2 Key M slot 22x80, PCIe Gen4 x4.

- **USB Interface**
  - Four USB ports on the rear I/O:
    - Two for USB 3.2 Gen2 in Type A
    - Two for USB 3.2 Gen2 in Type C with DisplayPort Alternate Mode supported
  - Two USB 2.0 ports in 2x5-pin internal wafer connector

- **Display**
  - Two DisplayPort. Max. resolution is 5120x3200 @60Hz in USB Type C.
  - One eDP. Max resolution is 5120x3200 @60Hz.
  - One HDMI2.0. Max. resolution is 4096x2160 @60Hz.
  - One HDMI1.4. Max. resolution is 4096x2160 @30Hz.

- **Watchdog Timer**
  - 1~255 seconds or minutes; up to 255 levels.

- **Ethernet**
  - LAN1: Intel® I219-LM supports 1000/100/10Mbps Gigabit/Fast Ethernet with Wake-on-LAN and PXE Boot ROM
  - LAN2: Intel® I226-V supports 2500/1000/100/10Mbps Gigabit/Fast Ethernet with Wake-on-LAN and PXE Boot ROM
  - LAN3: Intel® I226-V supports 2500/1000/100/10Mbps Gigabit/Fast Ethernet with Wake-on-LAN and PXE Boot ROM

- **Audio**
  - HD audio link without codec
  - 1x8-pin 1.0mm wafer HDA signal to support expansion audio board AX93A22

- **Expansion Interface**
  - One M.2 Key B slot 30x42/ 30x52
  - One M.2 Key E slot 22x30

- **Power Input**
  - One 2x2-pin connector
  - +12V only DC-in
  - AT auto power on function supported

- **Trusted Platform Module (TPM)**
  - Controller: ST ST33HTPH2X32AHD8 via SPI bus interface
  - Complies with TPM2.0 main and PC client specification

- **Power Management**
  - ACPI (Advanced Configuration and Power Interface)

- **Form Factor**
  - 3.5" form factor

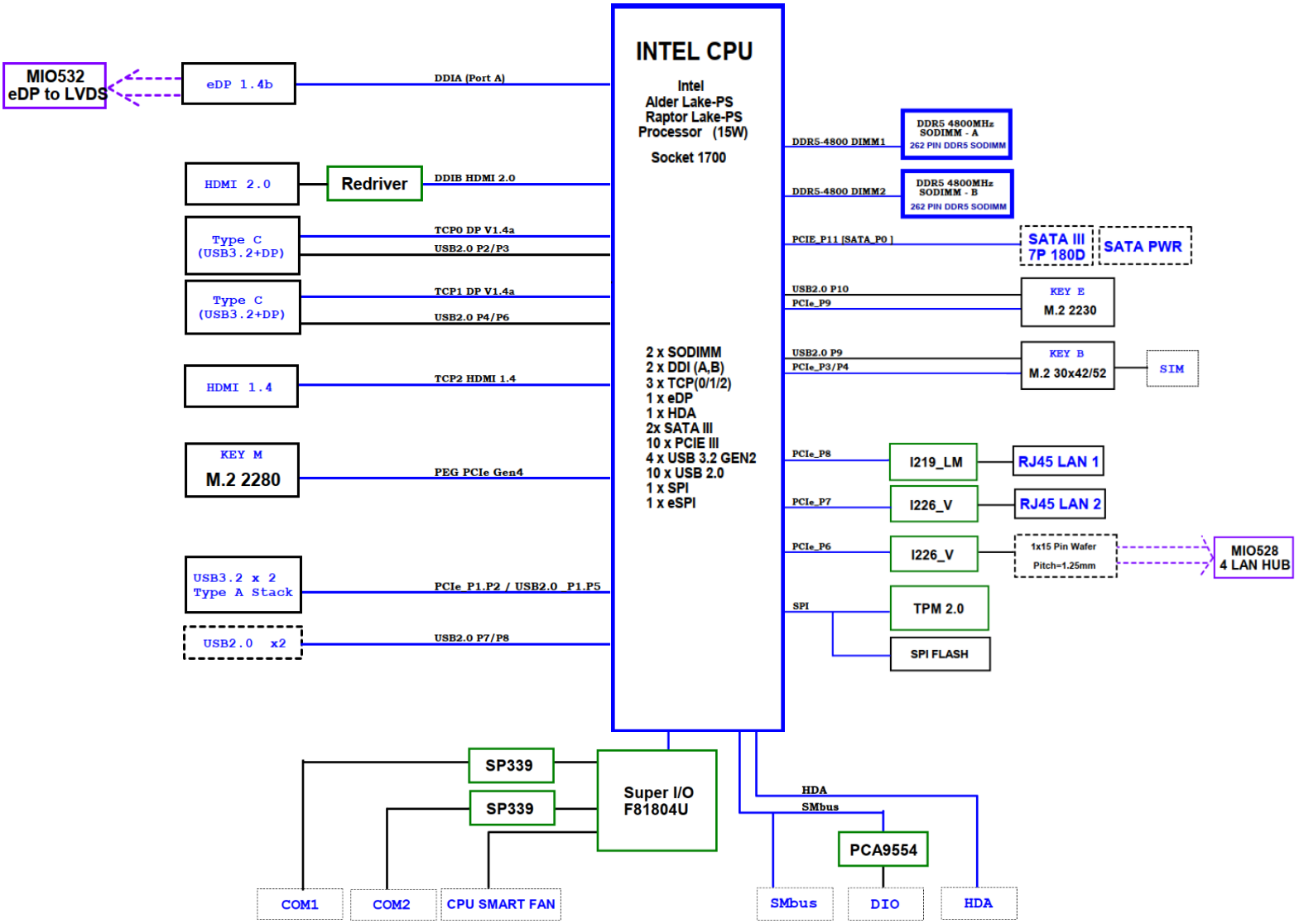
Note

All specifications and images are subject to change without notice.

1.3 Utilities

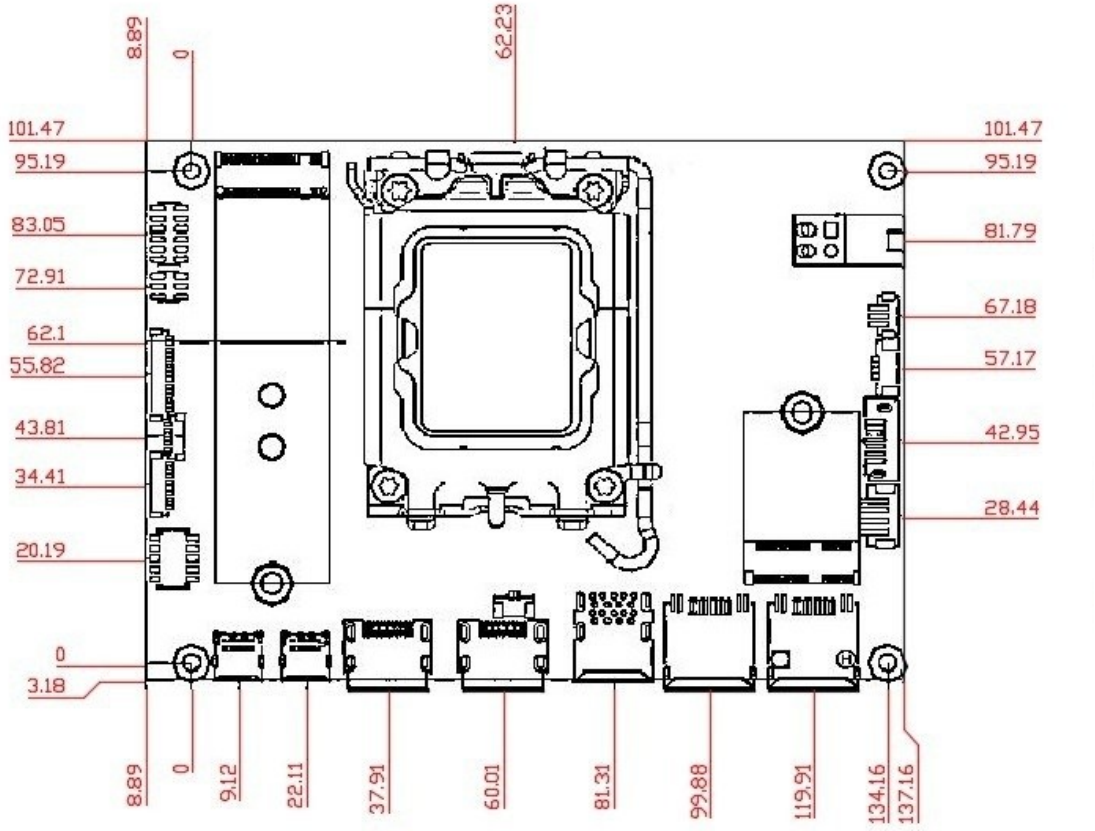
- Chipset and graphics driver
- Ethernet driver (Intel® I226 and i219)
- Audio driver (optional for AX93A22)
- Axiomtek eAPI3.0 SDK and Driver

1.4 Block Diagram

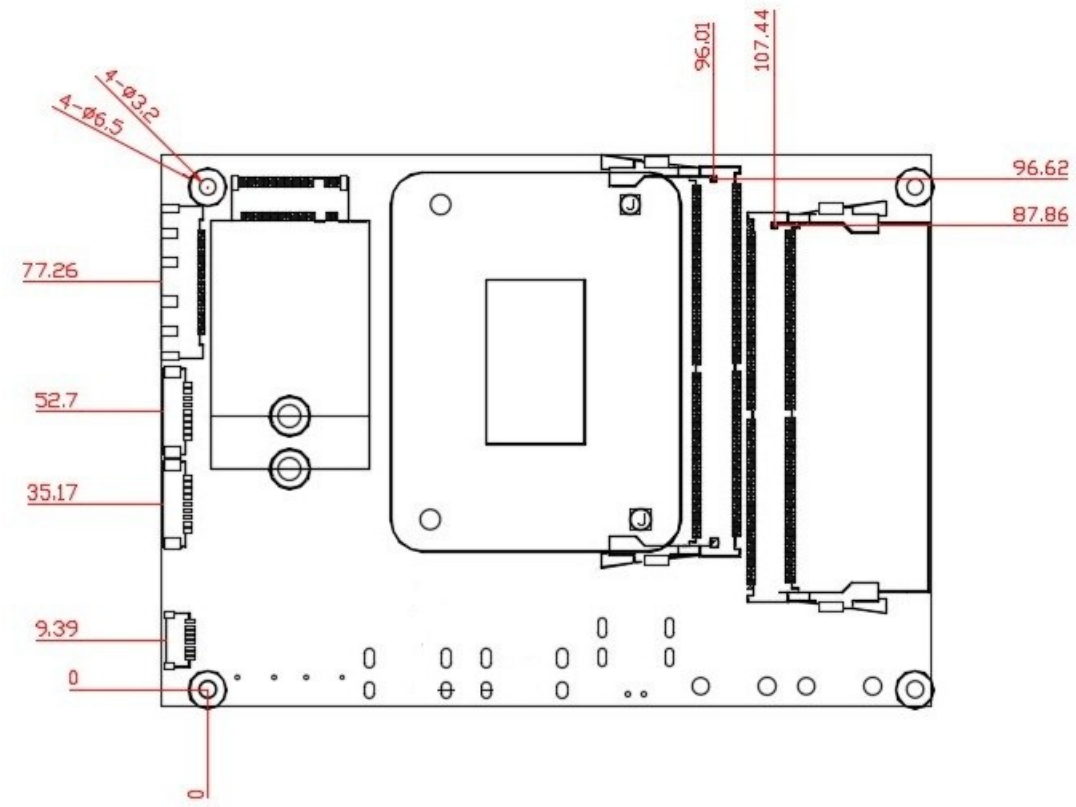


Section 2
Board and Pin Assignments

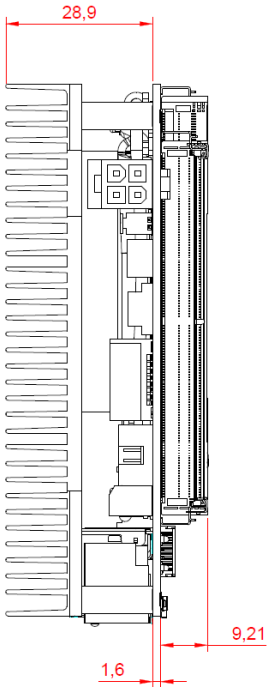
2.1 Board Dimensions and Fixing Holes



Top View

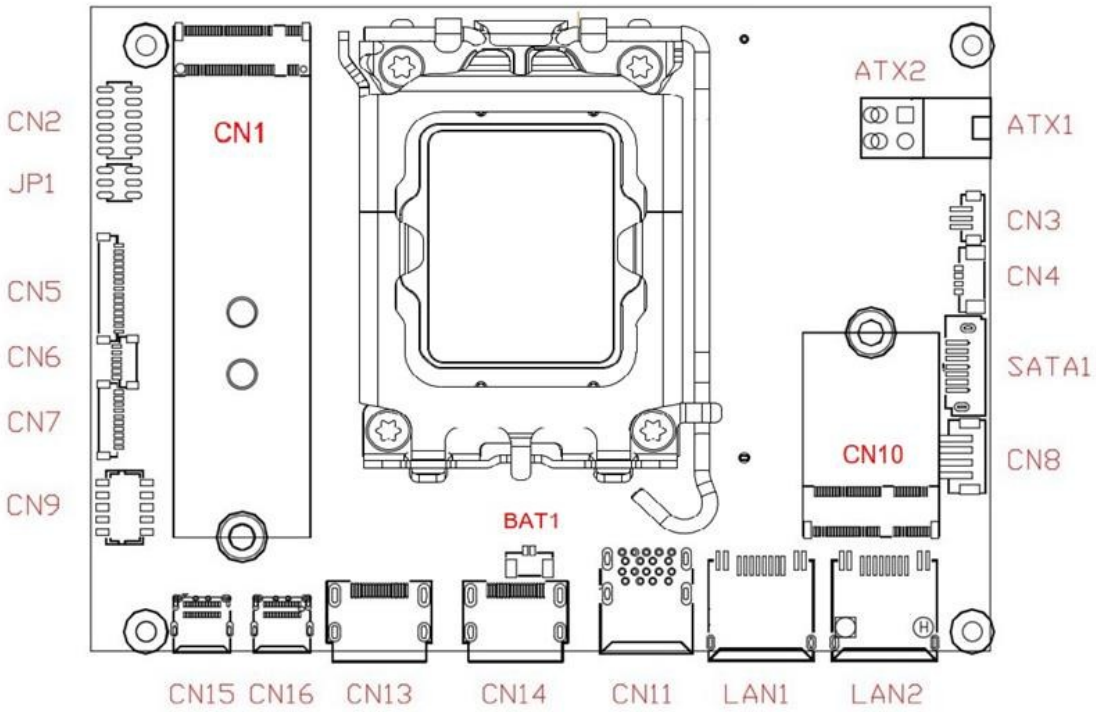


Bottom View

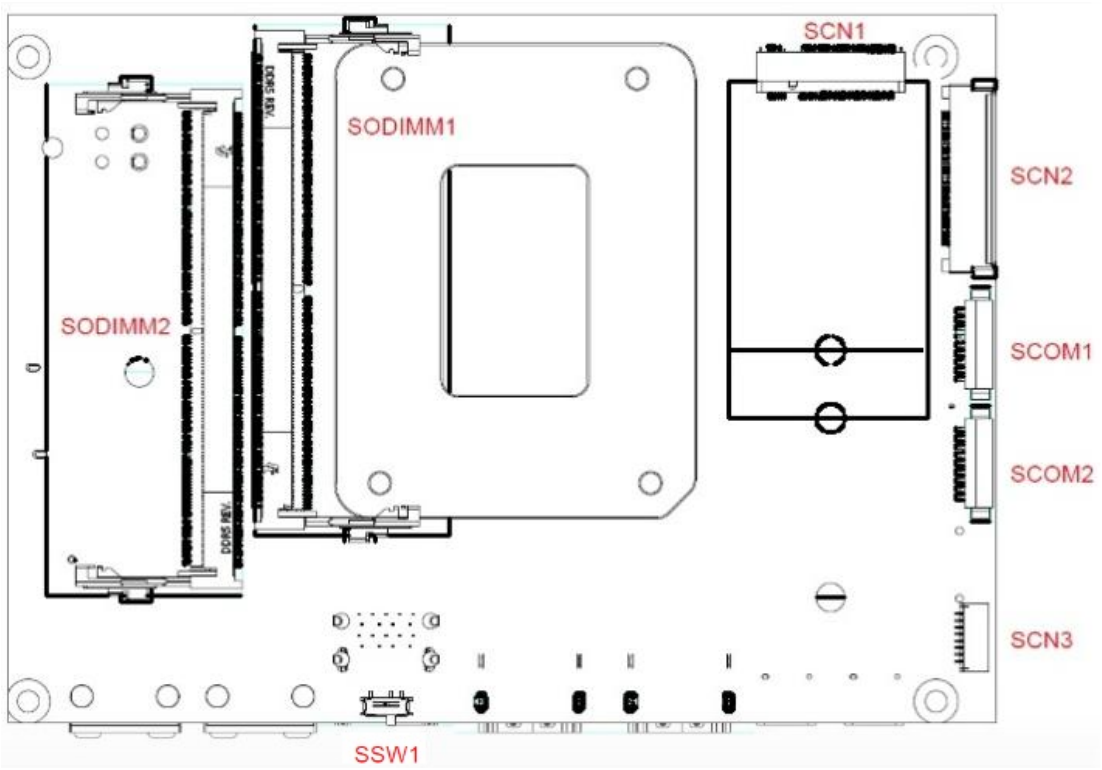


Side View

2.2 Board Layout



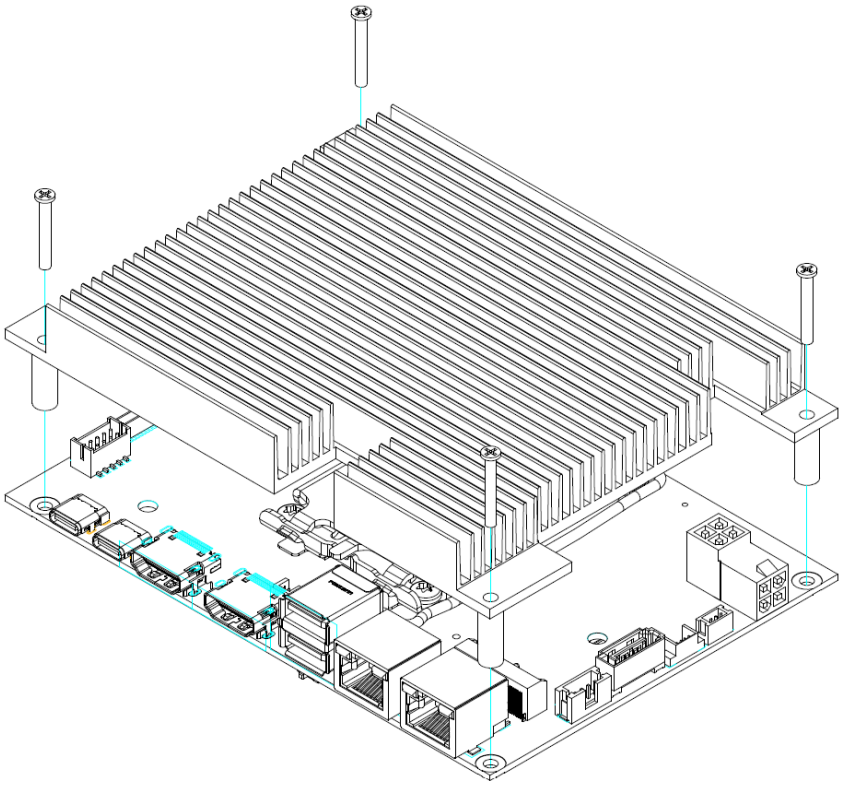
Top View



Bottom View

2.3 Installing Heatsink

The processor needs specially designed heatsink to cool down your system. After applying thermal grease on the processor and installing it on the socket, please place heatsink on top of the processor. Match the four screws to the fixing holes on the board. Then screw tightly the heatsink assembly onto the board.

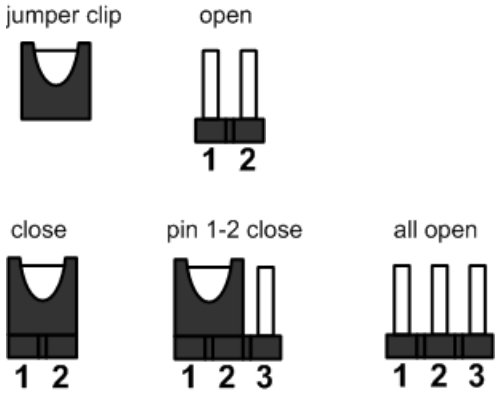


Note

Be careful not to over tighten the screws as it can damage the processor or the CPU board.

2.4 Jumper and Switch Settings

Jumper is a small component consisting of jumper clip and jumper pins. Install jumper clip on 2 jumper pins to close. And remove jumper clip from 2 jumper pins to open. Below illustration shows how to set up jumper.



Properly configure jumper and switch settings on the CAPA561 to meet your application purpose. Below you can find a summary table of jumper, switch and onboard default settings.

Note

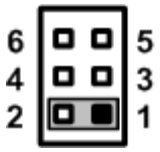
Once the default jumper or switch setting needs to be changed, please do it under power-off condition.

Jumper and Switch	Description	Setting
JP1	eDP BKL Control Default: +3.3V	1-2 Close
SSW1	Auto Power On Default: Disable	1-2 Close

2.4.1 eDP BKL Control (JP1)

This is a 2x3-pin jumper. Use JP1 to set eDP connector (SCN2) pin 1~4 to +3.3V, +5V or +12V.

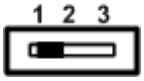
Function	Setting
+3.3V (Default)	1-2 close
+5V	2-4 close
+12V	5-6 close



2.4.2 Auto Power On (SSW1)

If SSW1 is enabled for power input, the system will be automatically power on without pressing soft power button. If SSW1 is disabled for power input, it is necessary to manually press soft power button to power on the system.

Function	Setting
Disable auto power on (Default)	1-2 close
Enable auto power on	2-3 close



2.5 Connectors

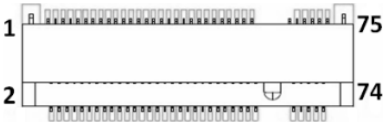
Signals go to other parts of the system through connectors. Loose or improper connection might cause problems, please make sure all connectors are properly and firmly connected. Here is a summary table of connectors on the hardware.

Connector	Description
CN1	M.2 Key M Connector
CN2	Front Panel Connector
CN3	Fan Wafer Connector
CN4	SMBus Wafer Connector
CN5	Ethernet (i225_6-V) Wafer Connector
CN6	SIM Card Wafer Connector
CN7	DIO Connector
CN8	SATA Power Connector
CN9	USB 2.0 Wafer Connector
CN10	M.2 Key E Connector
CN11	USB 3.2 Gen2 Type A Connector
CN13	HDMI 2.0 Connector
CN14	HDMI 1.4 Connector
CN15, CN16	USB 3.2 Type C Connectors
ATX1, ATX2	ATX Power Connectors
LAN1, LAN2	Ethernet Port 1 and 2
SATA1	SATA Connector
SCN1	M.2 Key B Connector
SCN2	eDP Connector
SCN3	HD Audio Wafer Connector
SCOM1, SCOM2	COM1 and COM2 Wafer Connectors
SODIMM1, SODIMM2	DDR5 SO-DIMM Connectors

2.5.1 M.2 Key M Connector (CN1)

The CN1 is an M.2 2280 Key M connector, supporting PCIe Gen4 x4 interface, recommended for installing NVMe storage cards.

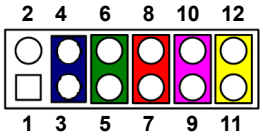
Pin	Signal	Pin	Signal
1	GND	2	+3.3V
3	GND	4	+3.3V
5	PCIE_RXN_3	6	NC
7	PCIE_RXP_3	8	NC
9	GND	10	TP1
11	PCIE_TXN_3	12	+3.3V
13	PCIE_TXP_3	14	+3.3V
15	GND	16	+3.3V
17	PCIE_RXN_2	18	+3.3V
19	PCIE_RXP_2	20	NC
21	GND	22	NC
23	PCIE_TXN_2	24	NC
25	PCIE_TXP_2	26	NC
27	GND	28	NC
29	PCIE_RXN_1	30	NC
31	PCIE_RXP_1	32	NC
33	GND	34	NC
35	PCIE_TXN_1	36	NC
37	PCIE_TXP_1	38	NC
39	GND	40	SMB_1P8_CLK
41	PCIE_RXN_0	42	SMB_1P8_DATA
43	PCIE_RXP_0	44	SMB_1P8_ALERT
45	GND	46	NC
47	PCIE_TXN_0	48	NC
49	PCIE_TXP_0	50	PERST#
51	GND	52	CLKREQ#
53	REF_CLK_N	54	PEWAKE#
55	REF_CLK_P	56	NC
57	GND	58	NC
59	**Key M**	60	**Key M**
61		62	
63		64	
65		66	
67	NC	68	SUSCLK
69	KEYM_PEDET	70	+3.3V
71	GND	72	+3.3V
73	GND	74	+3.3V
75	GND		



2.5.2 Front Panel Connector (CN2)

This is a 2x6-pin header (pitch=2.0mm) for front panel interface.

Pin	Signal	Pin	Signal
1	BUZZER-	2	BUZZER+
3	GND	4	PWR_PSON_N
5	GND	6	+5V
7	GND	8	PSIN+
9	GND	10	HW RST+
11	SATA_LED-	12	SATA_LED+3.3V



Internal Buzzer
Pin 1(-) and 2(+) connect the internal buzzer cable.

Power Status (PS-ON)
Pin 4 and pin 3 are PS-ON signal which are connected to know the power status of this board.

Power LED
Pin 6 connects anode (+) of LED and pin 5 connects cathode(-) of LED. The power LED lights up when the system is powered on.

Power On/Off Button
Pin 7 and 8 connect the power button on front panel to CPU board, which allows users to turn on or off power.

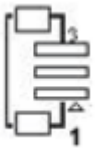
System Reset Switch
Pin 9 and 10 connect the case-mounted reset switch that reboots your computer without turning off the power switch. It is a better way to reboot your system for a longer life of system power supply.

HDD Activity LED
This connection is linked to hard drive activity LED on the control panel. LED flashes when HDD is being accessed. Pin 11 and 12 connect the hard disk drive to the front panel HDD LED, pin 9 is assigned as cathode(-) and pin 10 is assigned as anode(+).

2.5.3 Fan Wafer Connector (CN3)

This is a 3-pin (pitch=1.5mm) connector for fan interface. You can find fan speed option within BIOS Setup Utility if fan is installed. For further information, see BIOS Setup Utility: Advanced\H/W Monitor\PC Health Status (see section 4.4).

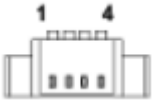
Pin	Signal
1	GND
2	Fan speed feedback
3	+12V



2.5.4 SMBus Wafer Connector (CN4)

This is a 4-pin (pitch=1.25mm) connector for SMBus interface. The SMBus (System Management Bus) is a simple bus for the purpose of lightweight communication.

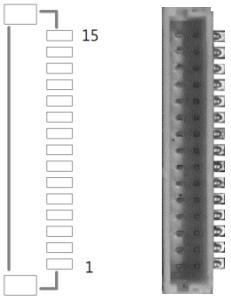
Pin	Signal
1	SMB_CLK
2	SMB_DAT
3	PLTRST
4	GND



2.5.5 Ethernet Wafer Connector (CN5)

This is a 15-pin wafer connector (pitch=1.0mm) for LAN3 Ethernet port interface.

Pin	Signal
1	GND
2	LED_ACT
3	+3.3VA
4	GND
5	DP0
6	DN0
7	DP1
8	DP2
9	DN2
10	DN1
11	DP3
12	DN3
13	PLTRST
14	LED_2500
15	LED_1000

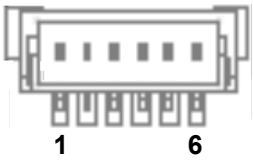


2.5.6 SIM Card Wafer Connector (CN6)

The CN6 is a 6-pin (pitch=1.0mm) wafer connector compliant with JST B6B-PH-K-S for SIM Card interface. To provide a SIM card slot, it is recommended to connect the AX93A19 to SCN1.

In order to work properly, the SIM card must be used together with 3G/4G/5G module in M.2 Key B connector (SCN1). It is mainly used in 3G/4G/5G cellular network application.

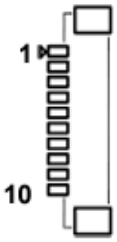
Pin	Signal
1	SIM_PWR
2	SIM_RESET
3	SIM_CLK
4	SIM_DAT
5	VPP
6	GND



2.5.7 DIO Connector (CN7)

This is a 10-pin (pitch=1.00mm) connector for DIO interface.

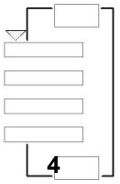
Pin	Signal
1	DIO0
2	DIO7
3	DIO1
4	DIO6
5	DIO2
6	DIO5
7	DIO3
8	DIO4
9	+5V
10	GND



2.5.8 SATA Power Connector (CN8)

The is a 4-pin (pitch=2.0mm) wafer connector fully compliant with JST B4B-PH-K-S.

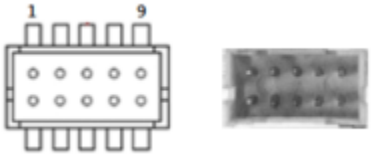
Pin	Signal
1	+12V Level
2	GND
3	GND
4	+5V Level



2.5.9 USB 2.0 Wafer Connector (CN9)

This is a 2x5-pin (pitch=2.0mm) wafer connector compliant with Hirose DF11-XDP-2DSA, for installing versatile USB 2.0 compliant interface peripherals.

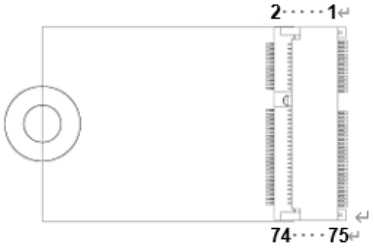
Pin	Signal	Pin	Signal
1	USB VCC (+5VA)	2	USB VCC (+5VA)
3	DN8	4	DN7
5	DP8	6	DP7
7	GND	8	GND
9	GND	10	GND



2.5.10 M.2 Key E Connector (CN10)

The CN10 is a M.2 2230 Key E connector. It is recommended to install the M.2 wireless module via PCIe Gen3 x1 and USB 2.0 with 22mm width x 30mm length.

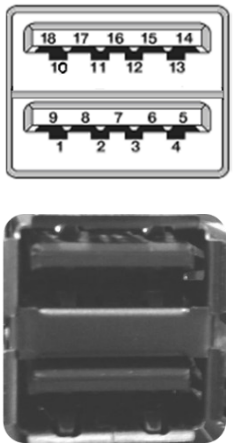
Pin	Signal	Pin	Signal
1	GND	2	+3.3V
3	USB_D+	4	+3.3V
5	USB_D-	6	NC
7	GND	8	NC
9	NC	10	NC
11	NC	12	NC
13	NC	14	NC
15	NC	16	NC
17	NC	18	GND
19	NC	20	UART_BT_WAKE_N
21	NC	22	UART2_BT_RXD
23	NC	24	**Key E**
25	**Key E**	26	
27		28	
29		30	
31		32	UART2_BT_TXD
33	GND	34	UART2_BT_CTS
35	PCIE_TX_P	36	UART2_BT_BTS
37	PCIE_TX_N	38	CL_RST
39	GND	40	CL_DATA
41	PCIE_RX_P	42	CL_CLK
43	PCIE_RX_N	44	NC
45	GND	46	NC
47	REF_CLK_P	48	NC
49	REF_CLK_N	50	SUSCLK
51	GND	52	PERST#
53	CLKREQ#	54	W_DISABLE2#
55	PEWAKE#	56	W_DISABLE1#
57	GND	58	I2C_DAT
59	NC	60	I2C_CLK
61	NC	62	ALERT#
63	GND	64	NC
65	NC	66	NC
67	NC	68	NC
69	GND	70	NC
71	NC	72	+3.3V
73	NC	74	+3.3V
75	GND		



2.5.11 USB 3.2 Gen2 Type A Connector (CN11)

The board comes with two Universal Serial Bus (compliant with USB 3.2 Gen 2 (10Gb/s)) ports on the rear I/O for installing USB peripherals such as keyboard, mouse, scanner, etc.

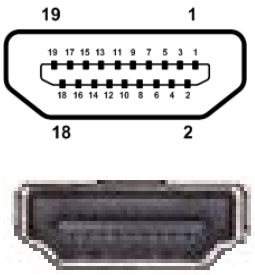
Pin	Signal	Pin	Signal
1	USB_VCC (+5V)	10	USB_VCC (+5V)
2	USB_DN1	11	USB_DN5
3	USB_DP1	12	USB_DP5
4	GND	13	GND
5	USB3_RXN0	14	USB3_RXN1
6	USB3_RXP0	15	USB3_RXP1
7	GND	16	GND
8	USB3_TXN0	17	USB3_TXN1
9	USB3_TXP0	18	USB3_TXP1



2.5.12 HDMI 2.0 Connector (CN13)

HDMI 2.0 supports up to 4K resolution at 60Hz, 32 audio channels, and 12-bit color depth. It ensures dynamic audio-video synchronization and is backward compatible with HDMI 1.4.

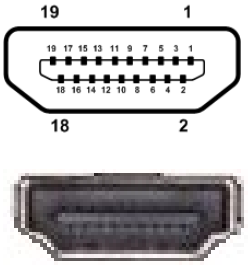
Pin	Signal	Pin	Signal
1	HDMI1 OUT_DATA2+	2	GND
3	HDMI1 OUT_DATA2-	4	HDMI1 OUT_DATA1+
5	GND	6	HDMI1 OUT_DATA1-
7	HDMI1 OUT_DATA0+	8	GND
9	HDMI1 OUT_DATA0-	10	HDMI1 OUT_Clock+
11	GND	12	HDMI1 OUT_Clock-
13	HDMI1_CEC	14	N.C
15	HDMI1 OUT_SCL	16	HDMI1 OUT_SDA
17	GND	18	+5V
19	HDMI1_HTPLG		



2.5.13 HDMI 1.4 Connector (CN14)

HDMI 1.4 supports 1080p video, 3D content, ARC, Ethernet and up to 8 audio channels. It is suitable for standard multimedia devices.

Pin	Signal	Pin	Signal
1	HDMI2 OUT_DATA2+	2	GND
3	HDMI2 OUT_DATA2-	4	HDMI2 OUT_DATA1+
5	GND	6	HDMI2 OUT_DATA1-
7	HDMI2 OUT_DATA0+	8	GND
9	HDMI2 OUT_DATA0-	10	HDMI2 OUT_Clock+
11	GND	12	HDMI2 OUT_Clock-
13	HDMI2_CEC	14	N.C
15	HDMI2 OUT_SCL	16	HDMI2 OUT_SDA
17	GND	18	+5V
19	HDMI2_HTPLG		

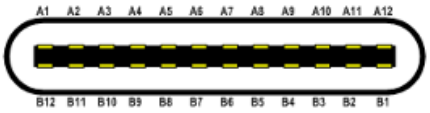


2.5.14 USB 3.2 Type C Connectors (CN15, CN16)

This Type-C port is capable of operating as a USB 3.2 interface and also supports DisplayPort Alternate Mode with maximum resolution to 5120x3200 @60Hz

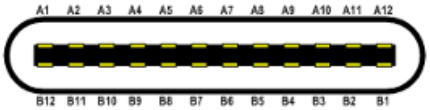
CN15:

Pin	Signal	Pin	Signal
A1	GND	B1	GND
A2	TCP1_TX0+	B2	TCP1_TX1+
A3	TCP1_TX0-	B3	TCP1_TX1+
A4	USB_VCC (+5V)	B4	USB_VCC (+5V)
A5	CC01	B5	CC02
A6	USB #4_D+	B6	USB #6_D+
A7	USB #4_D-	B7	USB #6_D-
A8	TCP1_SBU1	B8	TCP1_SBU2
A9	USB_VCC (+5V)	B9	USB_VCC (+5V)
A10	TCP1_RX1-	B10	TCP1_RX0-
A11	TCP1_RX1+	B11	TCP1_RX0+
A12	GND	B12	GND



CN16:

Pin	Signal	Pin	Signal
A1	GND	B1	GND
A2	TCP0_TX0+	B2	TCP0_TX1+
A3	TCP0_TX0-	B3	TCP0_TX1+
A4	USB_VCC (+5V)	B4	USB_VCC (+5V)
A5	CC11	B5	CC12
A6	USB #2_D+	B6	USB #3_D+
A7	USB #2_D-	B7	USB #3_D-
A8	TCP0_SBU1	B8	TCP0_SBU2
A9	USB_VCC (+5V)	B9	USB_VCC (+5V)
A10	TCP0_RX1-	B10	TCP0_RX0-
A11	TCP0_RX1+	B11	TCP0_RX0+
A12	GND	B12	GND

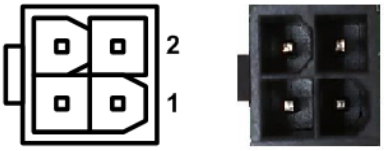


2.5.15 ATX Power Connector (ATX1, ATX2)

Steady and sufficient power can be supplied to all components on the board by connecting the power connector. Please make sure all components and devices are properly installed before connecting the power connector.

The ATX1 is a 90D 4-pin power connector and ATX2 is a 180D 4-pin power connector. Follow the connector orientation to plug the external power supply. Properly press down power supply plug until it completely and firmly fits into this connector. Loose connection may cause system instability. Note that ATX1 is co-lay and BOM optional.

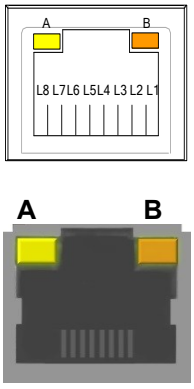
Pin	Signal
1	GND
2	GND
3	DC-In
4	DC-In



2.5.16 Ethernet Ports (LAN1, LAN2)

The board has two RJ-45 Ethernet connectors (LAN1 and LAN2). Connection can be established by plugging one end of the Ethernet cable into LAN2 and the other end (phone jack) to a 2500/1000/100/10-Base-T hub. Also, connection can be established by plugging one end of the Ethernet cable into LAN1 and the other end (phone jack) to a 1000/100/10-Base-T hub.

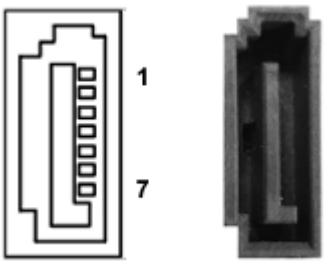
Pin	1000 Base-T	100/10 Base-T	Description
1	MDI0+	TX+	Bidirectional or Transmit Data+
2	MDI0-	TX-	Bidirectional or Transmit Data
3	MDI1+	RX+	Bidirectional or Receive Data+
4	MDI2+	N.C.	Bidirectional or Not Connected
5	MDI2-	N.C.	Bidirectional or Not Connected
6	MDI1-	RX-	Bidirectional or Receive Data-
7	MDI3+	N.C.	Bidirectional or Not Connected
8	MDI3-	N.C.	Bidirectional or Not Connected
A	Active Link LED Off: No link Blinking: Data activity detected		
B	Speed LED Green: 2500 Orange: 1000 OFF: 100/10		



2.5.17 SATA Connector (SATA1)

This Serial Advanced Technology Attachment (Serial ATA or SATA) connector is for high-speed SATA interface. It is a computer bus interface for connecting to devices such as hard disk drive.

Pin	Signal
1	GND
2	SATA_TX+
3	SATA_TX-
4	GND
5	SATA_RX-
6	SATA_RX+
7	GND



2.5.18 M.2 Key B Connector (SCN1)

The SCN1 is a M.2 Key B connector. It is recommended to install:

1. M.2 storage module with 22mm width x 42mm length when configuring to PCIe Gen3 x2
2. M.2 cellular module with 30mm width x 42mm length or 30mm width x 50/52mm length when configuring to PCIe Gen3 x1 and USB3.2.

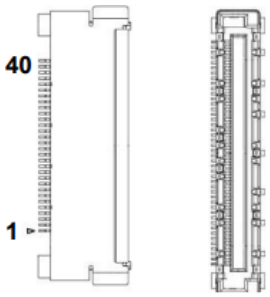
Pin	Signal	Pin	Signal
1	CONFIG_3	2	+3.3V_SBY
3	GND	4	+3.3V_SBY
5	GND	6	Full Card PWR OFF_SBY (+1.8V)
7	USB_DP9	8	W_DISABLE1#_SBY (+3.3V)
9	USB_DN9	10	NC
11	GND	12	**Key B**
13	**Key B**	14	
15		16	
17		18	
19		20	NC
21	CONFIG_0	22	NC
23	GPIO_11_SBY (+1.8V)	24	NC
25	NC	26	NC
27	GND	28	NC
29	PCIE1_RX_N /USB3_RX_N	30	SIM_RESET
31	PCIE1_RX_P /USB3_RX_P	32	SIM_CLK
33	GND	34	SIM_DATA
35	PCIE1_TX_N /USB3_TX_N	36	SIM_PWR
37	PCIE1_TX_P /USB3_TX_P	38	DEVSLP1
39	GND	40	SMB_CLK_SBY (+1.8V)
41	PCIE0_RX_N	42	SMB_DATA_SBY (+1.8V)
43	PCIE0_RX_P	44	SMB_ALERT_SBY (+1.8V)
45	GND	46	NC
47	PCIE0_TX_N	48	NC
49	PCIE0_TX_P	50	PERST#
51	GND	52	CLKREQ#
53	REF_CLK_N	54	PEWAKE#
55	REF_CLK_P	56	NC
57	GND	58	NC
59	NC	60	NC
61	NC	62	NC
63	NC	64	NC
65	NC	66	NC
67	RESET#_SBY (+1.8V)	68	SUSCLK
69	CONFIG_1	70	+3.3V_SBY
71	GND	72	+3.3V_SBY
73	GND	74	+3.3V_SBY
75	CONFIG_2		

Note ***It can be configured to support PCIex2 or USB3.2+PCIe via BIOS setting in section 4.4.***

2.5.19 eDP Connector (SCN2)

The eDP interface is available through 40-pin connector (SCN2), which is compliant with IPEX-20143. Pin 1~4 can be set to +3.3V, +5V or +12V with JP1 (see section 2.4.1).

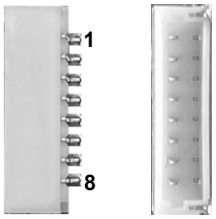
Pin	Signal	Pin	Signal
1	+DVCCM	21	eDP_TXN0
2	+DVCCM	22	eDP_TXP0
3	+DVCCM	23	GND
4	+DVCCM	24	eDP_AUX_DP
5	RST	25	eDP_AUX_DN
6	GND	26	GND
7	GND	27	GND
8	GND	28	GND
9	GND	29	GND
10	eDP_HPD#	30	GND
11	GND	31	eDP_BIST
12	eDP_TXN3	32	eDP_BLT_CTRL
13	eDP_TXP3	33	eDP_BLT_EN
14	GND	34	NC
15	eDP_TXN2	35	NC
16	eDP_TXP2	36	+12V_EDP_BKLT
17	GND	37	+12V_EDP_BKLT
18	eDP_TXN1	38	+12V_EDP_BKLT
19	eDP_TXP1	39	+12V_EDP_BKLT
20	GND	40	NC



2.5.20 HD Audio Wafer Connector (SCN3)

HD audio interface is available in an 8-pin (pitch=1.0mm) wafer connector fully compliant with JST BM08B-SRSS-TB. AX93A22 board is suggested to use in order to have Mic in/Line in and Line out.

Pin	Signal
1	+5VA
2	AUD_LINK_BCLK
3	AUD_LINK_SDI0
4	AUD_LINK_SDO
5	AUD_LINK_SYNC
6	AUD_LINK_RST
7	SLP_S3_N_BUF
8	GND

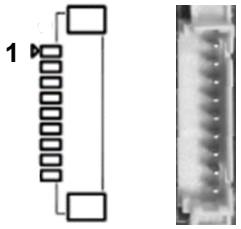


2.5.21 COM1 and COM2 Wafer Connectors (SCOM1, SCOM2)

These 9-pin (pitch=1.25mm) connectors are compliant with Molex 53047-0910. User is strongly recommended to use the matching cable 59380880250E. Both COM1 and COM2 support RS-232/422/485 by BIOS selecting (see section 4.4).

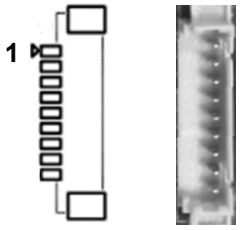
SCOM1:

Pin	RS-232	RS-422	RS-485
1	GND	GND	GND
2	RI1	No use	No use
3	DTR1	RX1-	No use
4	CTS1	No use	No use
5	TX1	RX1+	No use
6	RTS1	No use	No use
7	RX1	TX1+	Data+
8	DSR1	No use	No use
9	DCD1	TX1-	Data-



SCOM2:

Pin	RS-232	RS-422	RS-485
1	GND	GND	GND
2	RI2	No use	No use
3	DTR2	RX2-	No use
4	CTS2	No use	No use
5	TX2	RX2+	No use
6	RTS2	No use	No use
7	RX2	TX2+	Data+
8	DSR2	No use	No use
9	DCD2	TX2-	Data-



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Section 3
Hardware Description

3.1 Microprocessors

The CAPA561 supports Intel® Core™ i7/ i5/ i3/ Celeron® processors, which enable your system to operate under Windows® 11/10 and Linux environments. The system performance depends on the microprocessor. Make sure all correct settings are arranged for your installed microprocessor to prevent the CPU from damages.

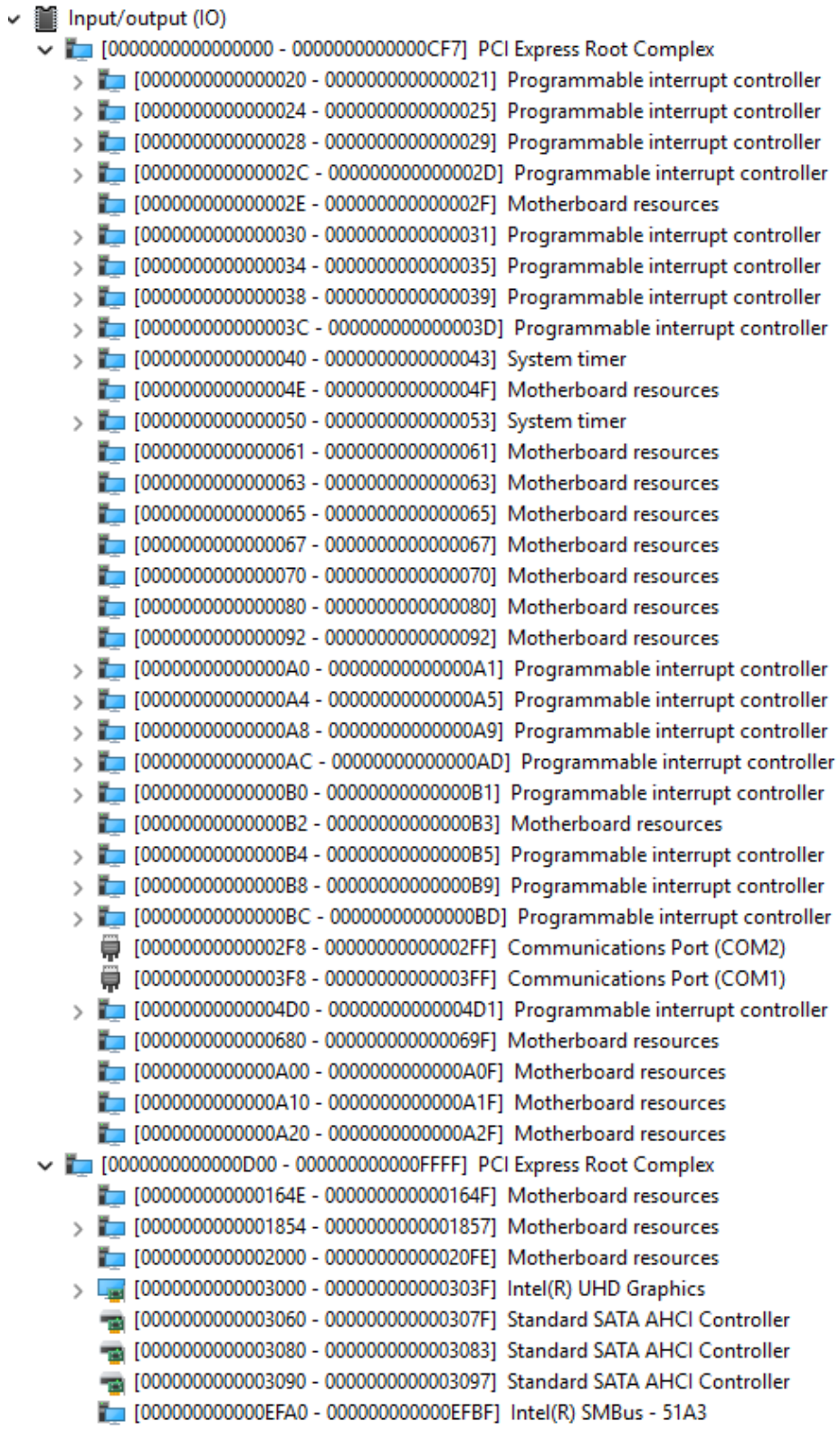
3.2 BIOS

The CAPA561 uses AMI Plug and Play BIOS with a single 512Mbit SPI Flash.

3.3 System Memory

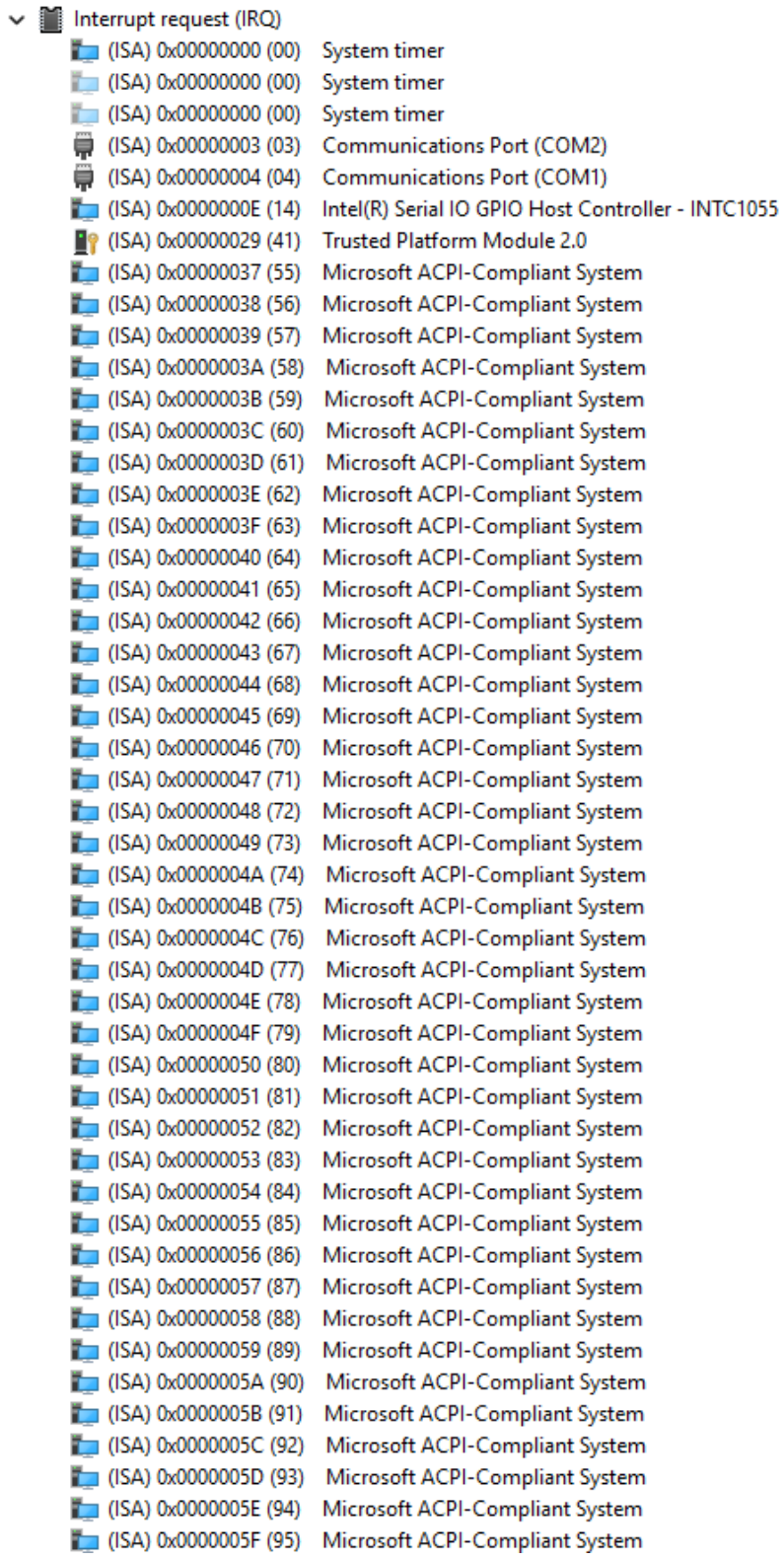
The CAPA561 supports two 262-pin DDR5 SO-DIMM sockets for maximum memory capacity up to 64GB DDR5 4800MHz. The memory module comes in sizes of 1GB, 2GB, 4GB , 8GB , 16GB,and 32GB.

3.4 I/O Port Address Map



3.5 Interrupt Controller (IRQ) Map

The interrupt controller (IRQ) mapping list is shown as follows:



(ISA) 0x00000060 (96) Microsoft ACPI-Compliant System
(ISA) 0x00000061 (97) Microsoft ACPI-Compliant System
(ISA) 0x00000062 (98) Microsoft ACPI-Compliant System
(ISA) 0x00000063 (99) Microsoft ACPI-Compliant System
(ISA) 0x00000064 (100) Microsoft ACPI-Compliant System
(ISA) 0x00000065 (101) Microsoft ACPI-Compliant System
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(PCI) 0x00000025 (37) Intel(R) Serial IO SPI Host Controller - 51AB
(PCI) 0x00000028 (40) Intel(R) Serial IO I2C Host Controller - 51E9
(PCI) 0xFFFFFFE5 (-27) Intel(R) Management Engine Interface #1
(PCI) 0xFFFFFFE6 (-26) Intel(R) USB 3.10 eXtensible Host Controller - 1.20 (Microsoft)
(PCI) 0xFFFFFFE7 (-25) Intel(R) USB 3.20 eXtensible Host Controller - 1.20 (Microsoft)
(PCI) 0xFFFFFFE8 (-24) Intel(R) UHD Graphics
(PCI) 0xFFFFFFE9 (-23) Intel(R) Ethernet Controller I226-V #2
(PCI) 0xFFFFFFEA (-22) Intel(R) Ethernet Controller I226-V #2
(PCI) 0xFFFFFFEB (-21) Intel(R) Ethernet Controller I226-V #2
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(PCI) 0xFFFFFFF2 (-14) Intel(R) Ethernet Controller I226-V
(PCI) 0xFFFFFFF3 (-13) Intel(R) Ethernet Connection (16) I219-LM
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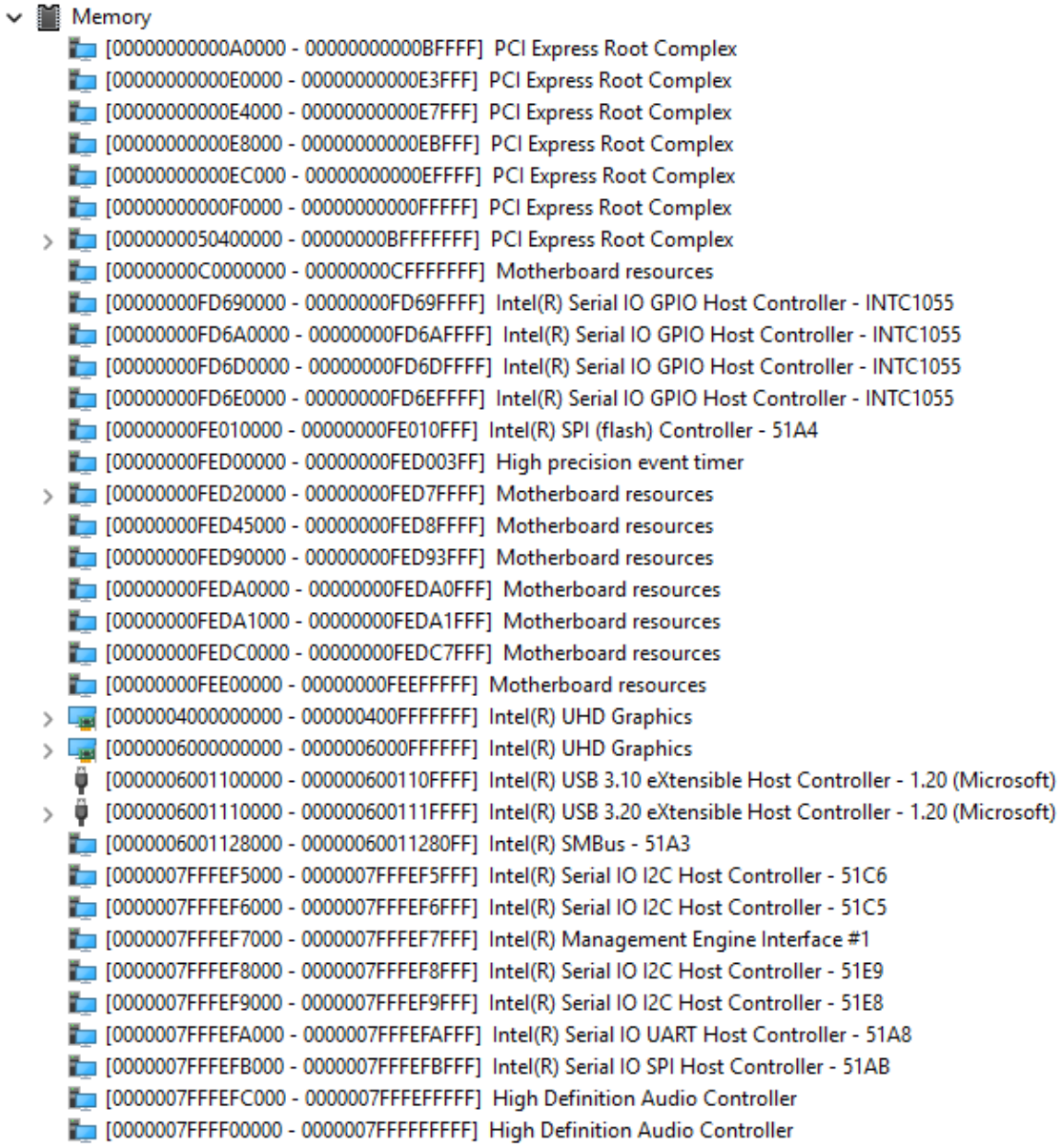
(PCI) 0xFFFFFFFA (-6) Standard NVM Express Controller
(PCI) 0xFFFFFFFB (-5) Standard SATA AHCI Controller
(PCI) 0xFFFFFFFC (-4) Intel(R) PCI Express Root Port #7 - 51BE
(PCI) 0xFFFFFFFD (-3) Intel(R) PCI Express Root Port #6 - 51BD
(PCI) 0xFFFFFFFE (-2) Intel(R) PCIe RC 060 (x4) G4 - A74D

3.6 Memory Map

The memory mapping list is shown as follows:



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Section 4
AMI BIOS Setup Utility

The AMI UEFI BIOS provides users with a built-in setup program to modify basic system configuration. All configured parameters are stored in a flash chip to save the setup information whenever the power is turned off. This section provides users with detailed description about how to set up basic system configuration through the AMI BIOS setup utility.

4.1 Starting

To enter the setup screens, follow the steps below:

1. Turn on the computer and press the <Del> key immediately.
2. After you press the <Del> key, the main BIOS setup menu displays. You can access the other setup screens from the main BIOS setup menu, such as the Advanced and Chipset menus.

It is strongly recommended that you should avoid changing the chipset's defaults. Both AMI and your system manufacturer have carefully set up these defaults that provide the best performance and reliability.

4.2 Navigation Keys

The BIOS setup/utility uses a key-based navigation system called hot keys. Most of the BIOS setup utility hot keys can be used at any time during the setup navigation process. These keys include <F1>, <F2>, <Enter>, <ESC>, <Arrow> keys, and so on.

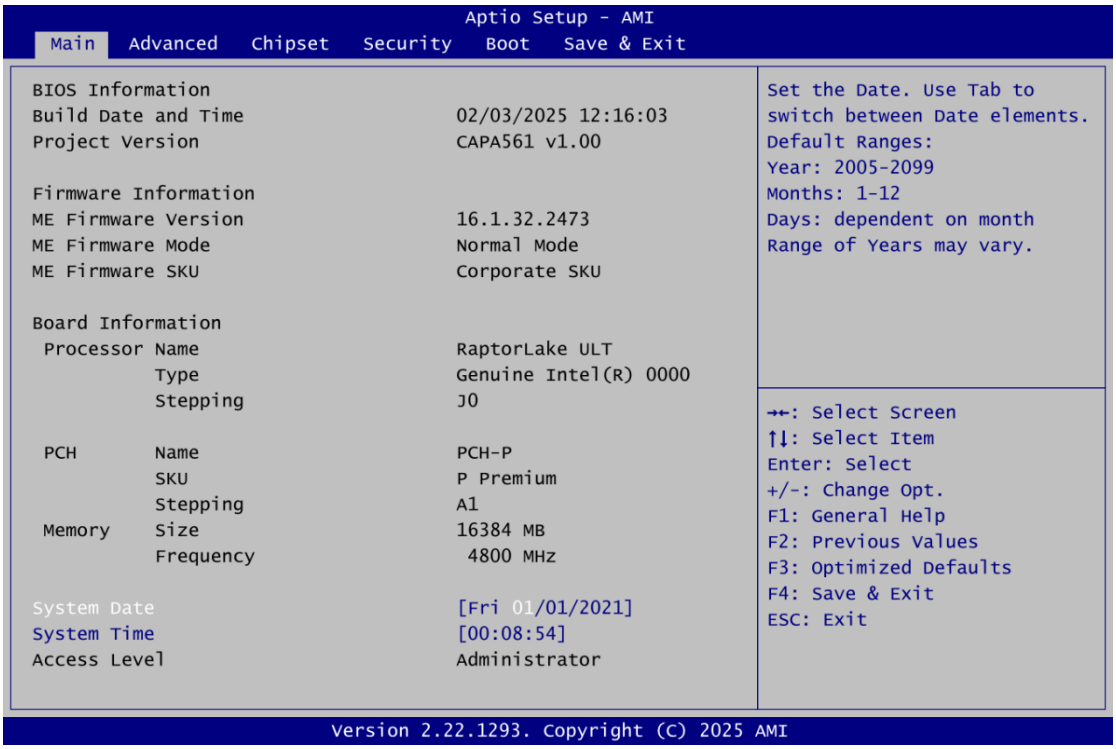
Note

Some of the navigation keys differ from one screen to another.

Hot Keys	Description
→← **Left/Right**	The Left and Right <Arrow> keys allow you to select a setup screen.
↑↓ **Up/Down**	The Up and Down <Arrow> keys allow you to select a setup screen or sub-screen.
+– Plus/Minus	The Plus and Minus <Arrow> keys allow you to change the field value of a particular setup item.
Tab	The <Tab> key allows you to select setup fields.
F1	The <F1> key allows you to display the General Help screen.
F2	The <F2> key allows you to Load Previous Values.
F3	The <F3> key allows you to Load Optimized Defaults.
F4	The <F4> key allows you to save any changes you have made and exit Setup. Press the <F4> key to save your changes.
Esc	The <Esc> key allows you to discard any changes you have made and exit the Setup. Press the <Esc> key to exit the setup without saving your changes.
Enter	The <Enter> key allows you to display or change the setup option listed for a particular setup item. The <Enter> key can also allow you to display the setup sub- screens.

4.3 Main Menu

When you first enter the setup utility, you will enter the Main setup screen. You can always return to the Main setup screen by selecting the Main tab. System Time/Date can be set up as described below. The Main BIOS setup screen is shown below.



- **BIOS/Firmware/Board Information**
  Display BIOS/Firmware/Board information.

- **System Date/Time**
  Use this option to change the system time and date. Highlight System Time or System Date using the <Arrow> keys. Enter new values through the keyboard. Press the <Tab> key or the <Arrow> keys to move between fields. The date must be entered in MM/DD/YY format. The time is entered in HH:MM:SS format.

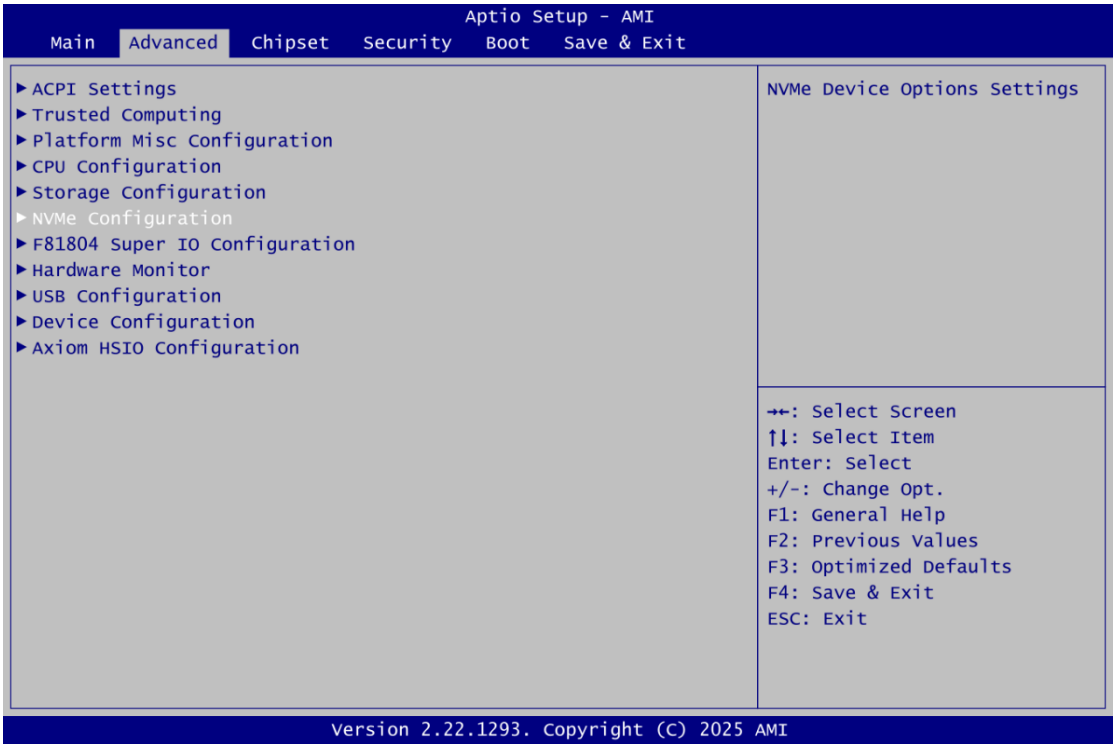
- **Access Level**
  Display the access level of current user.

4.4 Advanced Menu

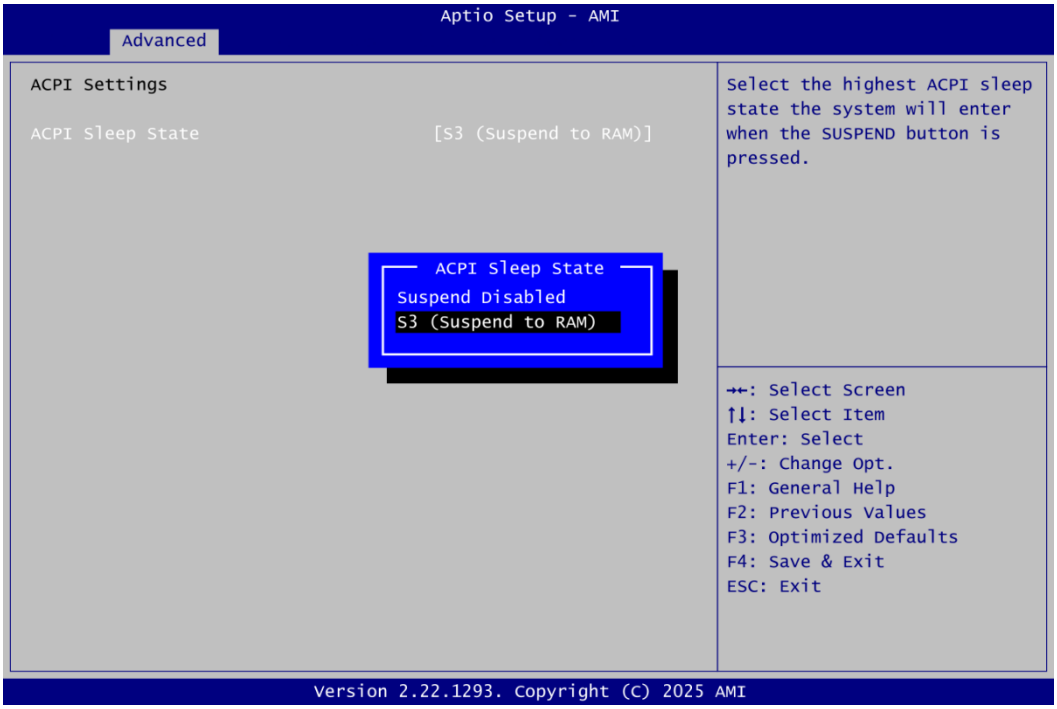
The Advanced menu also allows users to set configuration of the CPU and other system devices. You can select any of the items in the left frame of the screen to go to the sub menus:

- ACPI Settings
- Trusted Computing
- Platform Misc Configuration
- CPU Configuration
- Storage Configuration
- NVMe Configuration
- F81804 Super IO Configuration
- Hardware Monitor
- USB Configuration
- Device Configuration
- Axiom HSIO Configuration

For items marked with "►", please press <Enter> for more options.

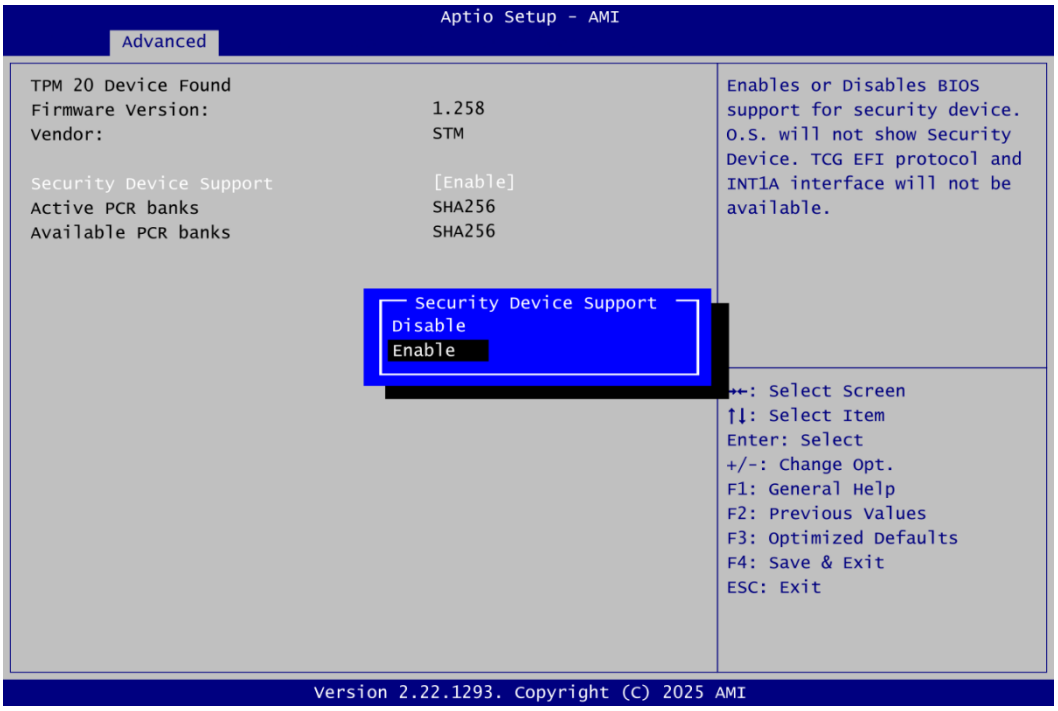


- **ACPI Settings**
  You can use this screen to select options for the ACPI configuration, and change the value of the selected option. A description of the selected item appears on the right side of the screen.



ACPI Sleep State
Select S3 (Suspend to RAM) as ACPI sleep state, the system will enter when suspend button is pressed.

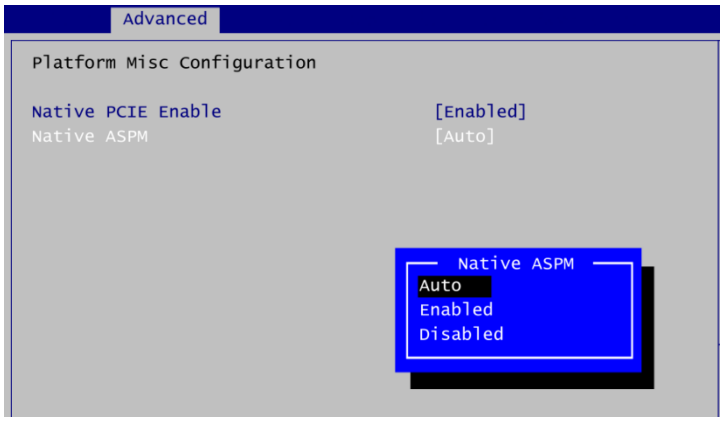
- **Trusted Computing**
  This screen provides function for specifying the TPM settings.



Security Device Support
Enable or disable BIOS support for security device, typically a TPM. When enabled (default setting), the BIOS initializes and makes the TPM available for use by the operating system and other system components. When disabled, the TPM is effectively hidden from the OS, and critical security functions, such as secure boot and disk encryption, may not function. Additionally, TCG EFI protocols and the INT1A interface, which are used for secure boot and other trusted computing tasks, will not be available.

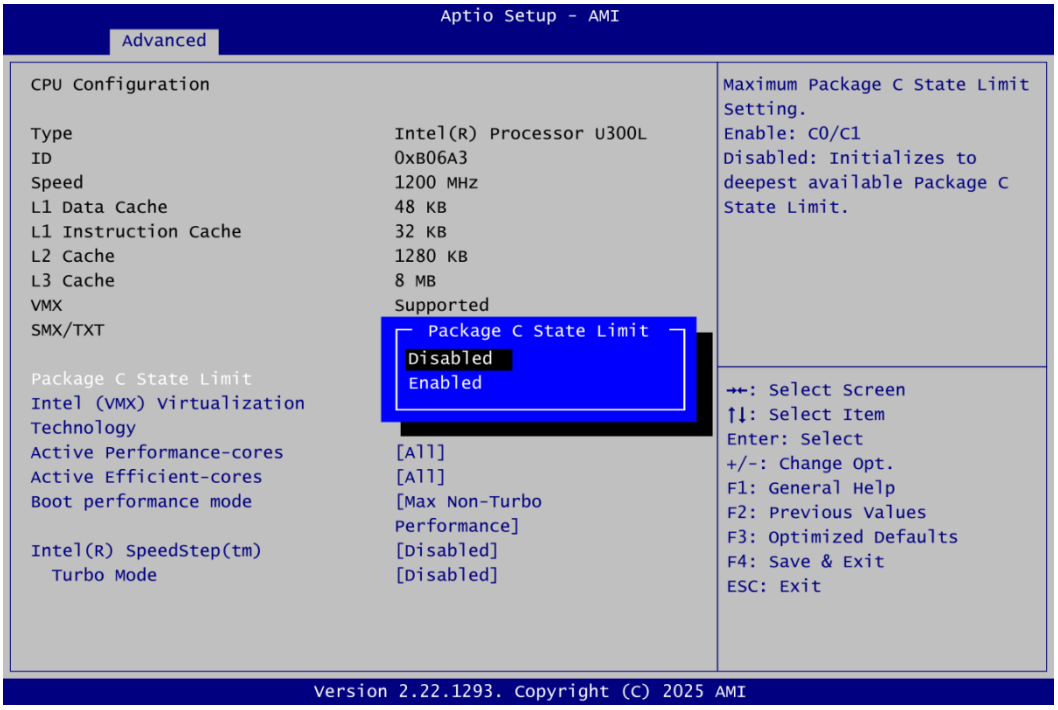
- **Platform Misc Configuration**
  Use this screen to configure platform-related features.

Native PCIE Enable
Enable or disable OS to control below features: Hot Plug, SHPC Native Hot Plug control, Power Management Events, PCIe Advanced Error Reporting control, PCIe Capability Structure control and Latency Tolerance Reporting control.



Native ASPM
This item allows OS to control PCIe Active-state power management (ASPM) features. If enabled, OS will control ASPM features of PCIe devices. If disabled, BIOS will control ASPM.

- **CPU Configuration**
  This screen shows the CPU Configuration, and you can change the value of the selected option.



Package C State Limit
Maximum Package C State Limit Setting. Enabled: C0\C1. Disabled: Initializes to deepest available Package C State Limit.

Intel (VMX) Virtualization Technology
Enable or disable Intel Virtualization Technology. When enabled, a VMM (Virtual Machine Mode) can utilize the additional hardware capabilities. It allows a platform to run multiple operating systems and applications independently, hence enabling a single computer system to work as several virtual systems.

Active Performance-cores
Number of P-cores to enable in each processor package. Note: Number of Cores and E-cores are looked at together. When both are {0,0}, P code will enable all cores.

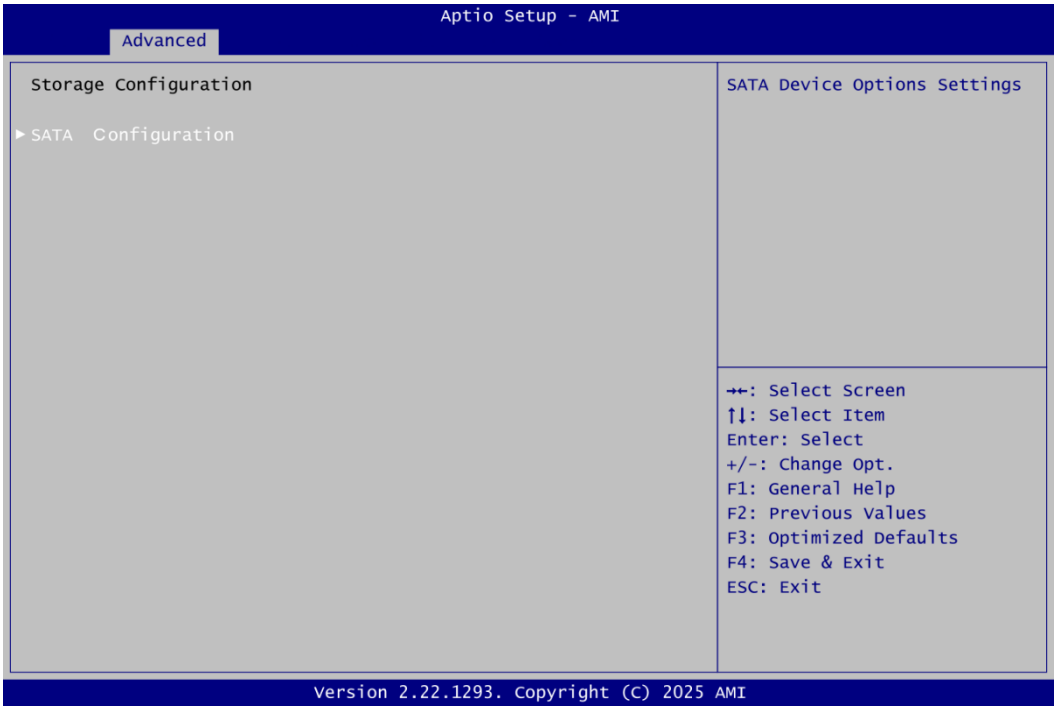
Active Efficient-cores
Number of E-cores to enable in each processor package. Note: Number of Cores and E-cores are looked at together. When both are {0,0}, P code will enable all cores.

Boot performance mode
Select the performance state that the BIOS will set starting from reset vector. The options are:
- Max Battery
- Max Non-Turbo Performance
- Turbo Performance

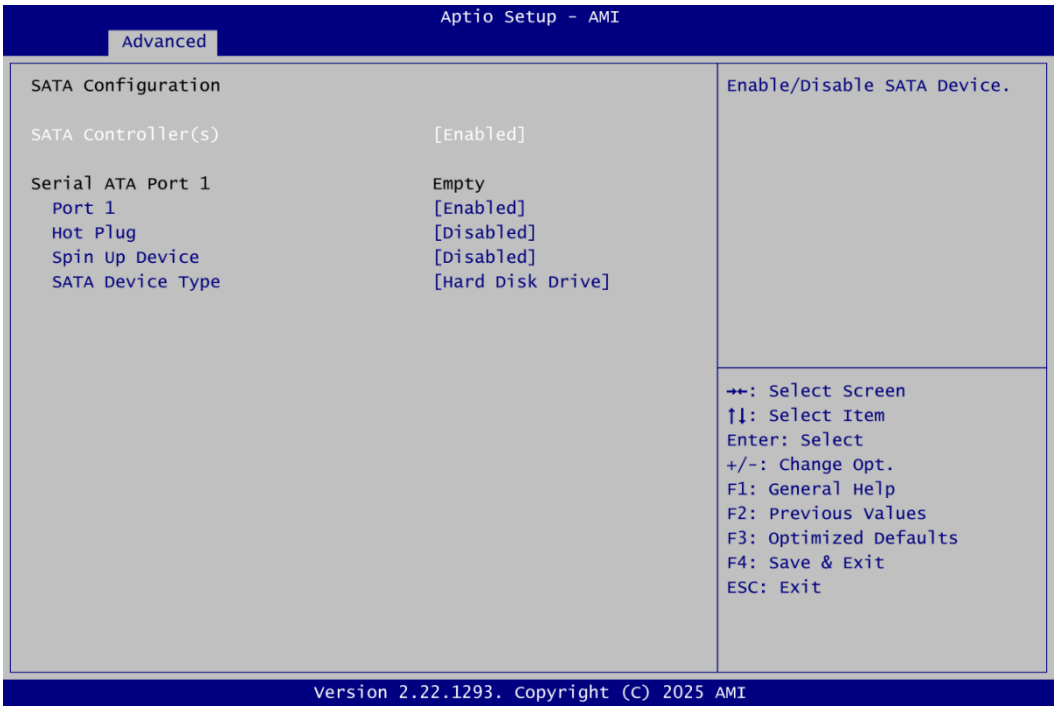
Intel(R) SpeedStep(tm)
Allows more than two frequency ranges to be supported.

Turbo Mode
Enable or disable processor Turbo Mode (requires EMTTM enabled too).

- **Storage Configuration**
  In the Storage Configuration menu, you can see the currently installed hardware in the SATA port. During system boot up, the BIOS automatically detects the presence of installed devices.



SATA Configuration
Click to open SATA device setting sub-screen.



SATA Controller(s)
Enable or disable the SATA Controller feature.

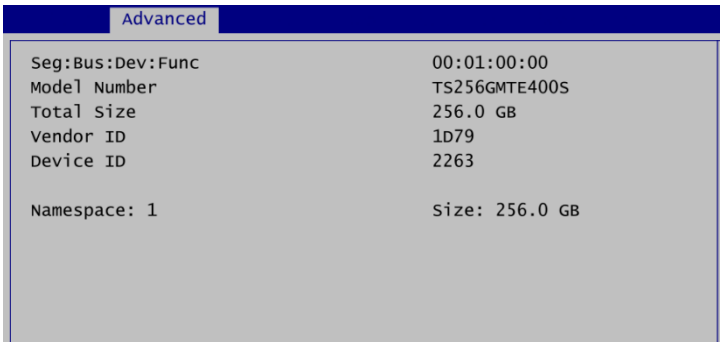
Port 1
Enable or disable SATA port.

Hot Plug
Designates this port as Hot Pluggable.

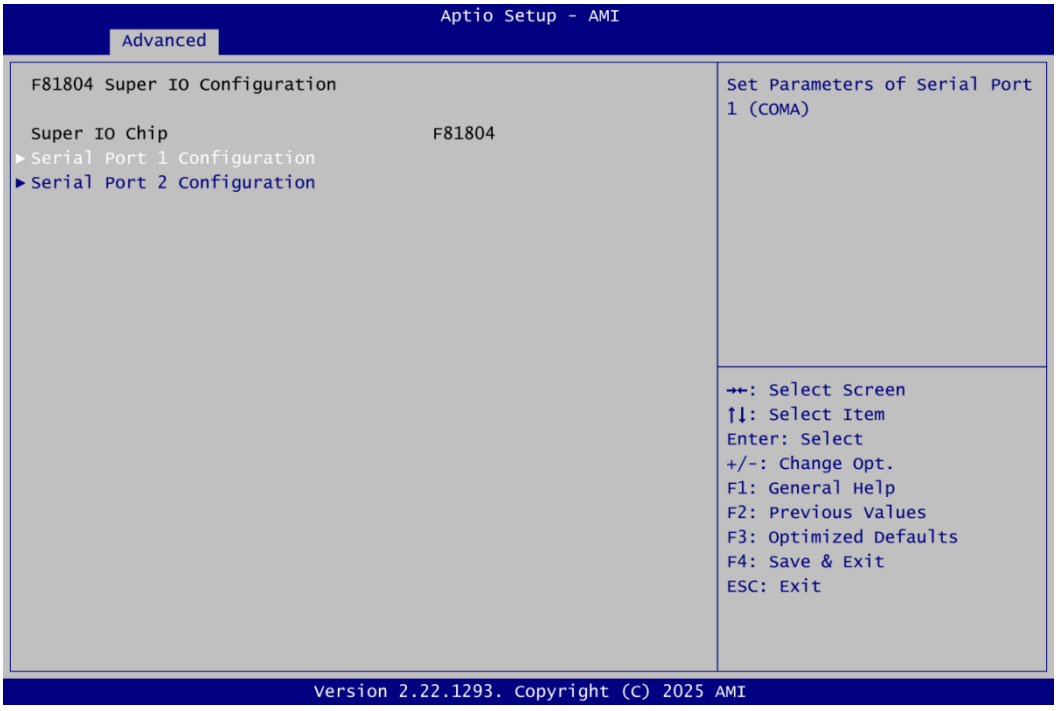
Spin Up Device
If enabled for any of ports Staggerred Spin Up will be performed and only the drives which have this option enabled will spin up at boot. Otherwise all drives spin up at boot.

SATA Device Type
Identify the SATA port is connected to Solid State Drive or Hard Disk Drive.

- **NVMe Configuration**
  This screen shows related information and settings for NVMe (Non-Volatile Memory Express) storage device.

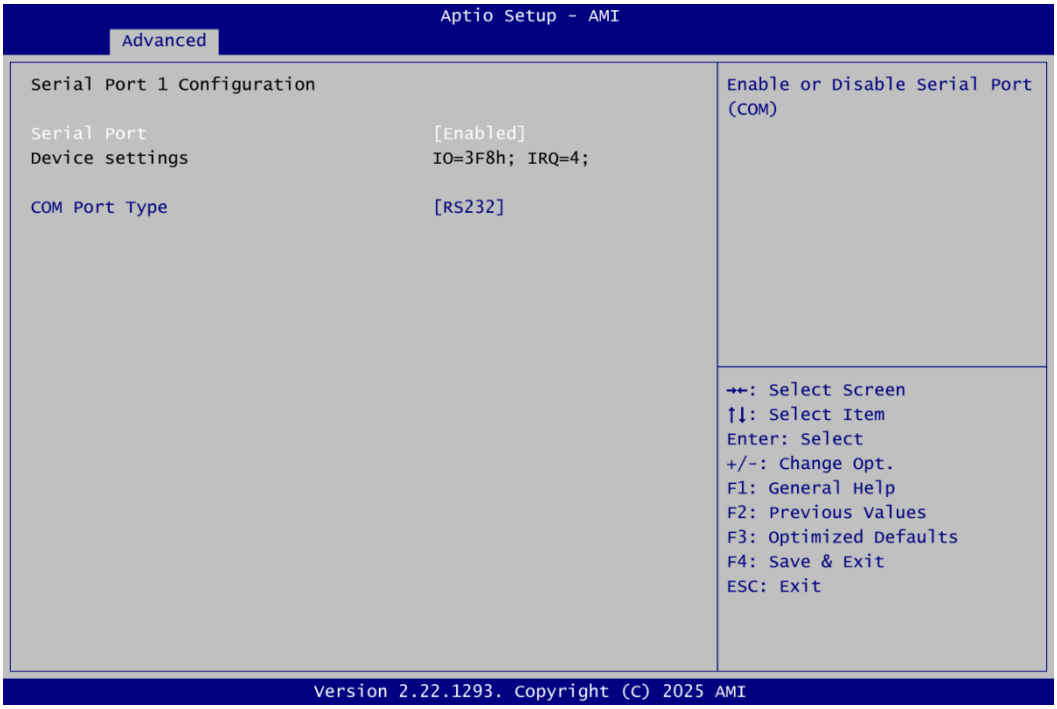


- **F81804 Super IO Configuration**
  You can use this screen to select options for Serial Port configuration, and change the value of the selected option. A description of the selected item appears on the right side of the screen. For items marked with "▶", please press <Enter> for more options.

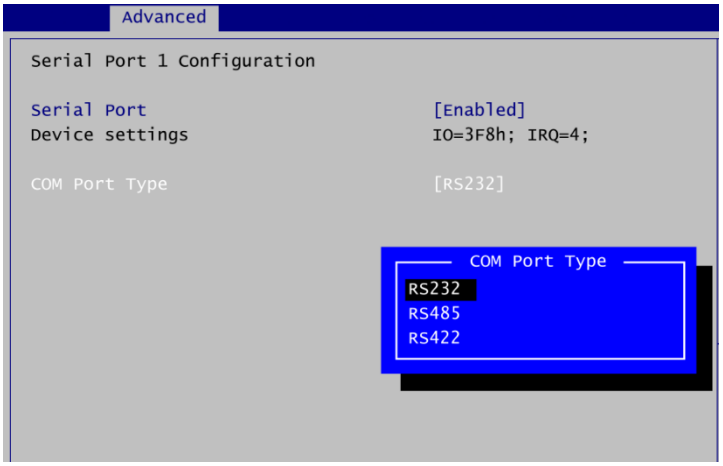


Serial Port 1~2 Configuration
Use this item to set parameters related to serial port 1~2.

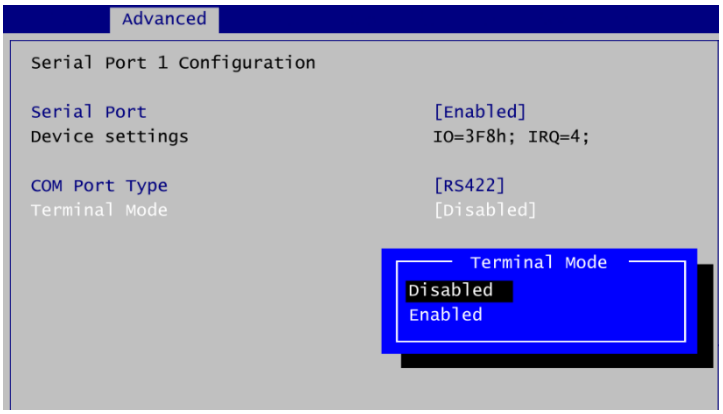
- **Serial Port 1 Configuration**



Serial Port
Enable or disable serial port 1. The optimal setting for onboard F81804 SIO address is 3F8h and for interrupt request address is IRQ4.

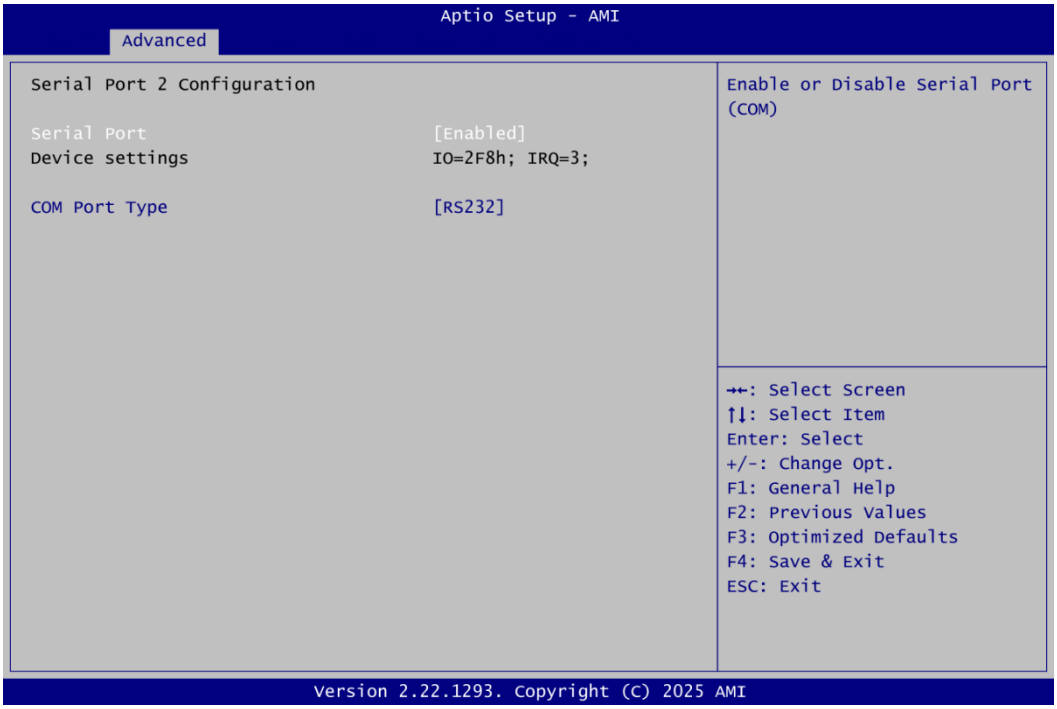


COM Port Type
Use this item to set RS-232/422/485 communication mode.



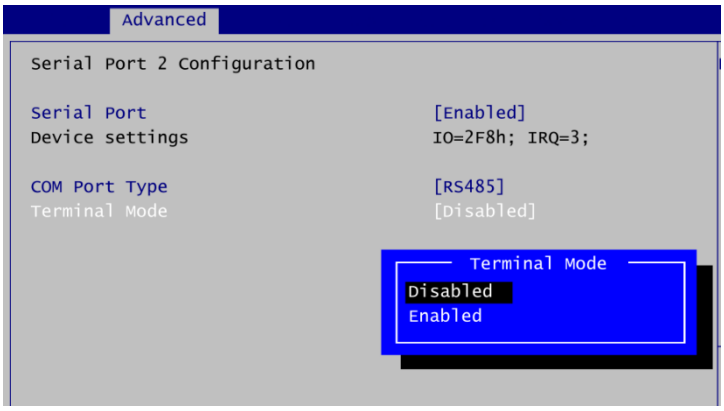
Terminal Mode
Enable terminal mode to enable the RS-422/485 termination resistor to enhance the signal.

- **Serial Port 2 Configuration**



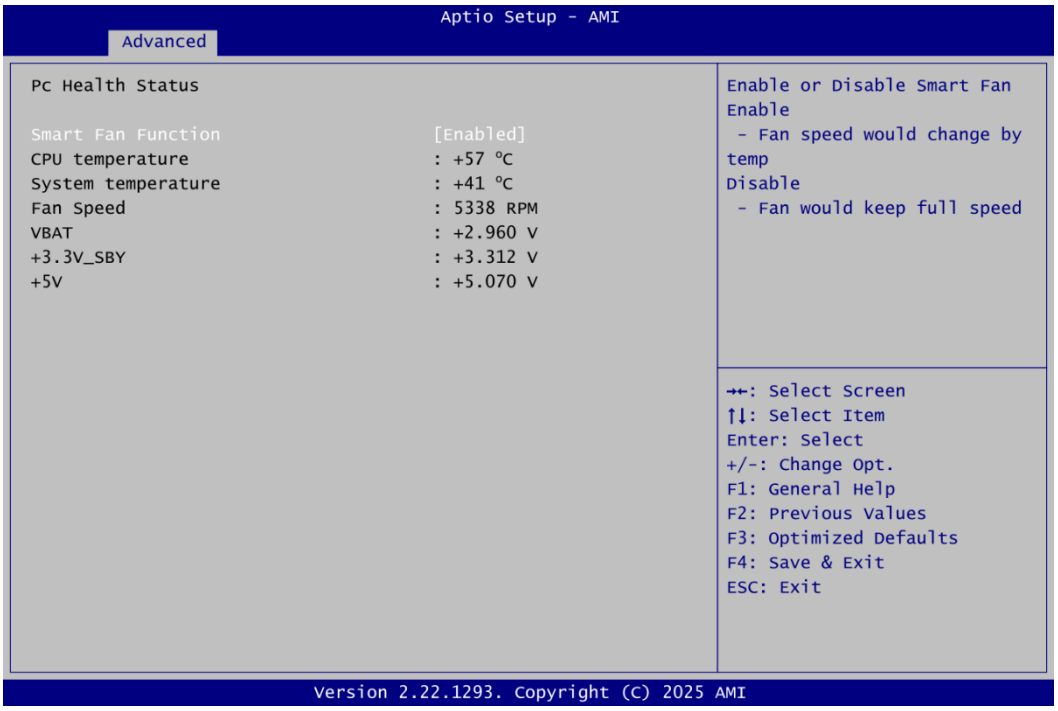
Serial Port
Enable or disable serial port 2. The optimal setting for onboard F81804 SIO address is 2F8h and for interrupt request address is IRQ3.

COM Port Type
Use this item to set RS-232/422/485 communication mode.



Terminal Mode
Enable terminal mode to enable the RS-422/485 termination resistor to enhance the signal.

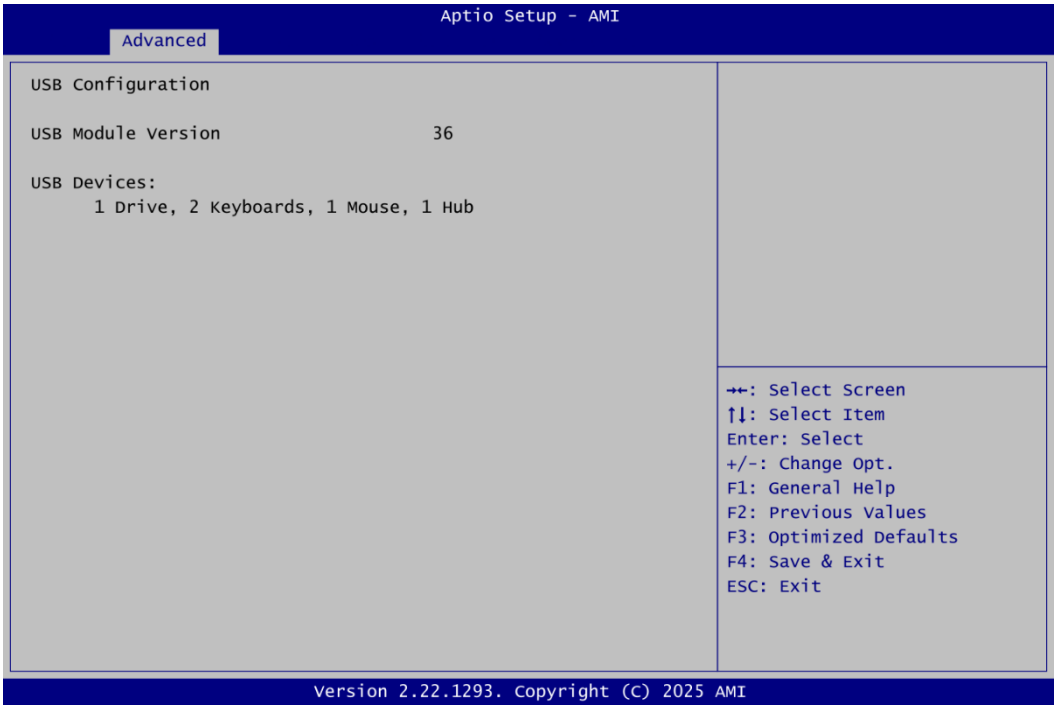
- **Hardware Monitor**
  This screen monitors hardware health status.



This screen displays the temperature of system and CPU, fan speed in RPM and system voltages (VBAT, +3.3V_SBY and +5V).

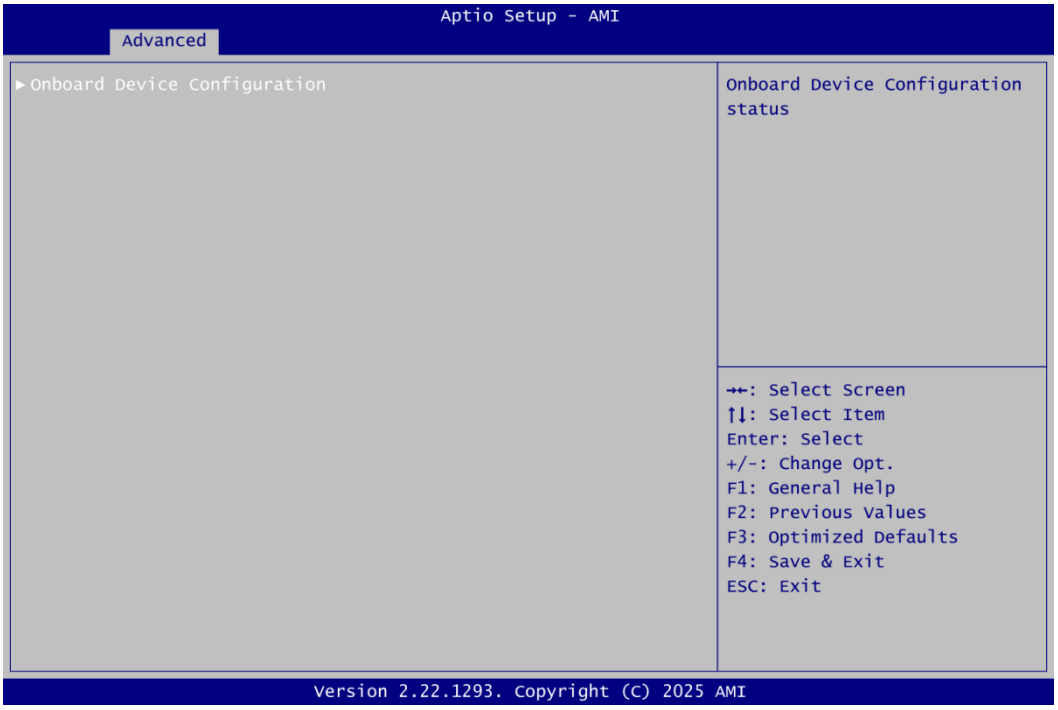
Smart Fan Function
Enable or disable Smart Fan control function.
- Enable: Fan speed would change according to temperature. The higher the temperature, the faster the fan spins.
- Disable: The fan always runs at full speed.
- The default setting is Enabled.

- **USB Configuration**



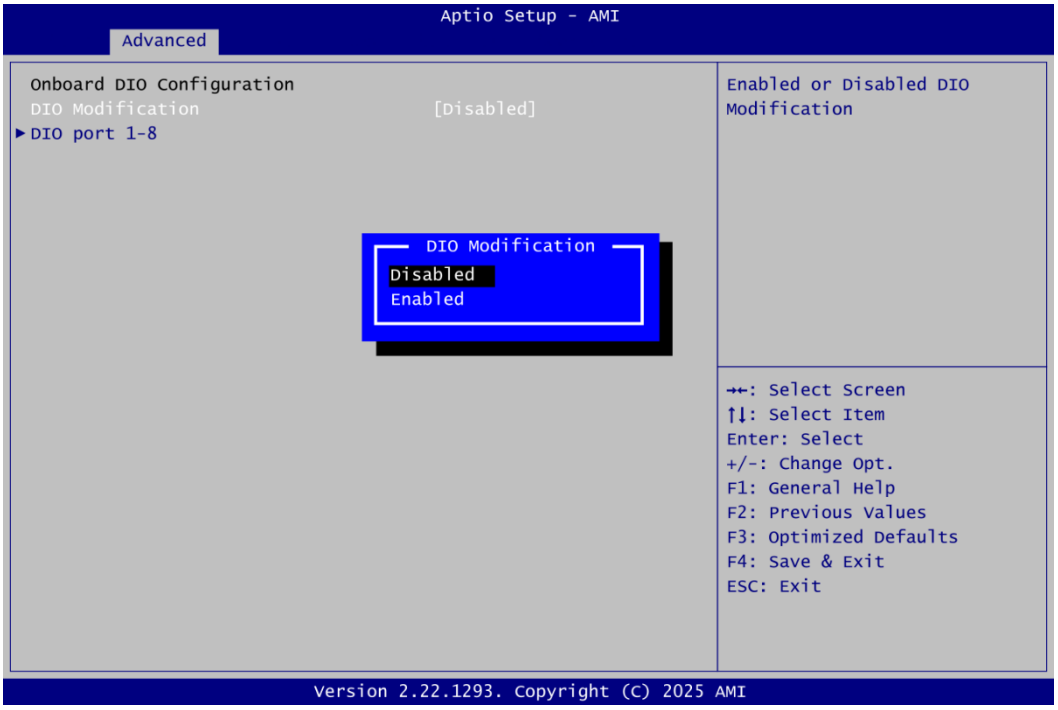
USB Devices
Display all detected USB devices.

- **Device Configuration**
  A description of the selected item appears on the right side of the screen. For items marked with "►", please press <Enter> for more options.



Onboard Device Configuration
Use this option to configure onboard device (e.g., Digital I/O setting).

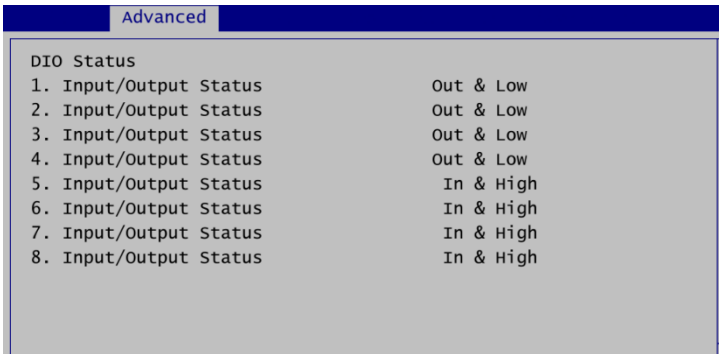
- **Onboard DIO Configuration**
  You can use this screen to select options for DIO configuration. A description of selected item appears on the right side of the screen.



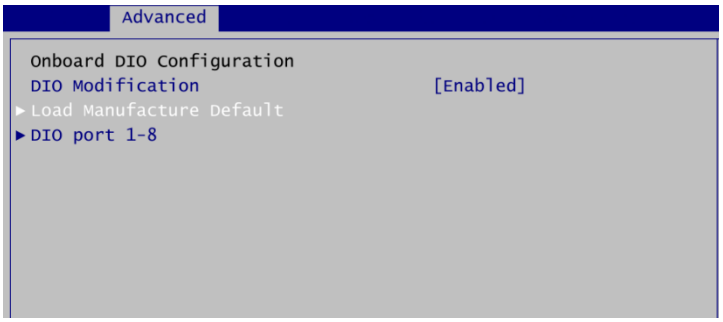
DIO Modification
Enable or disable digital I/O modification. The default is Disabled.

DIO port 1-8
Click on this option to open DIO status sub-screen.

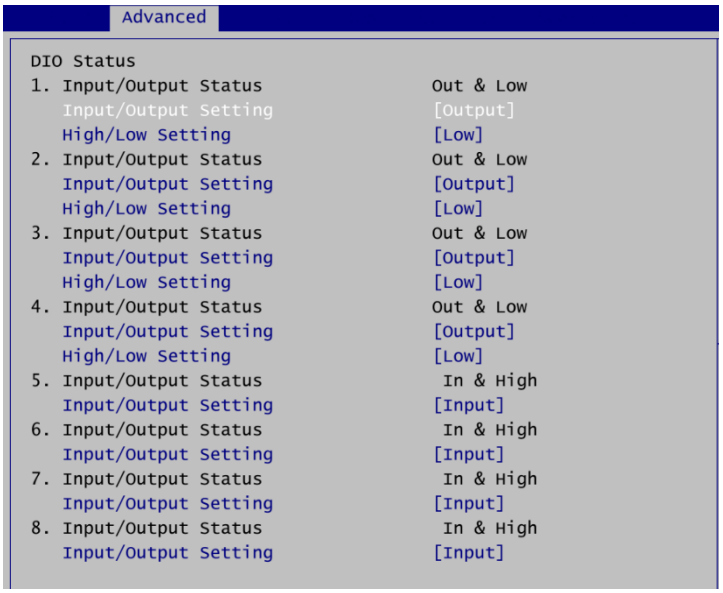
If DIO Modification is disabled, you are not allowed to change inputs/outputs setting. The DIO status sub screen is as follows:



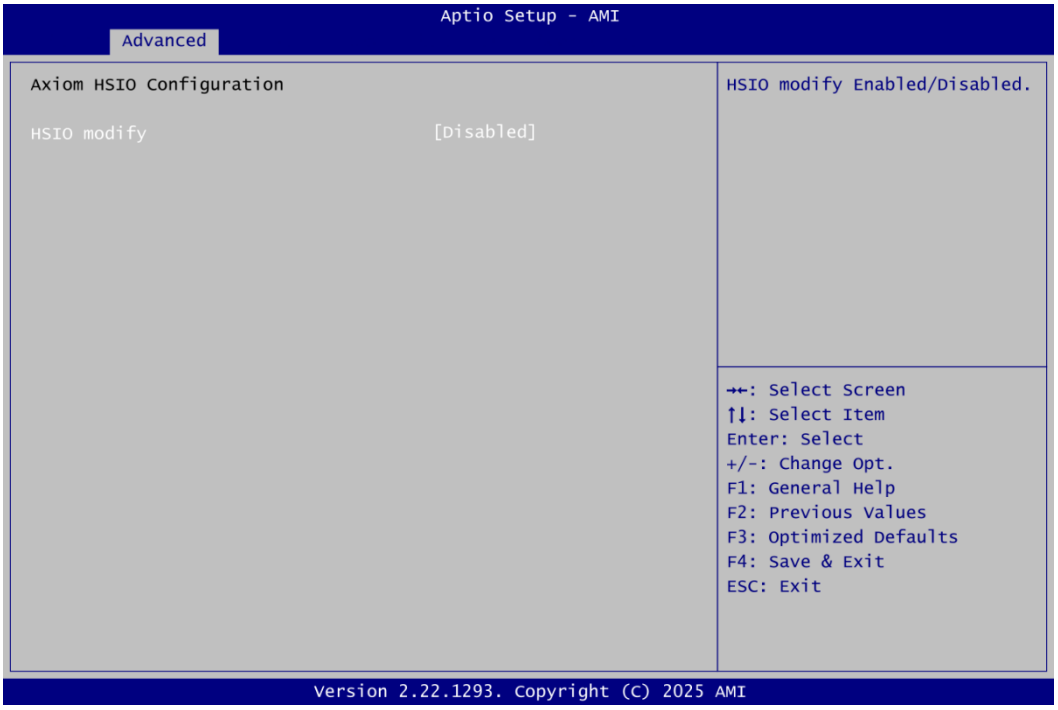
If DIO Modification is enabled, you can load manufacture default and access to the DIO status sub screen to change inputs/outputs setting, see images below.



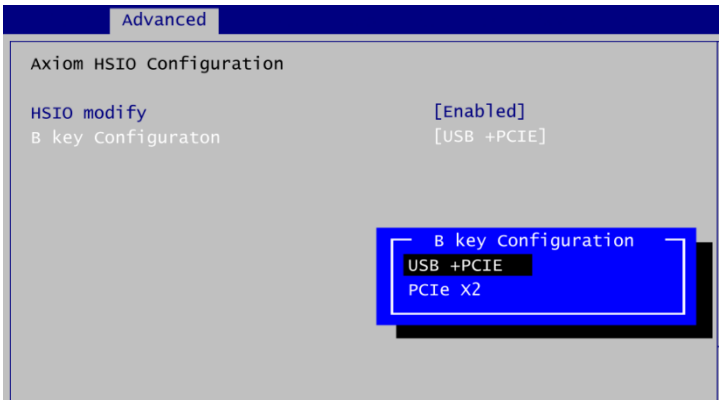
The DIO status sub-screen is as follows:



- **Axiom HSIO Configuration**
  Use this screen to set parameters related to Axiom High-Speed Input/Output configuration which refers to M.2 Key B Connector (see section 2.5.18)



HSIO modify
Enable or disable HSIO (High-Speed Input/Output) modify.

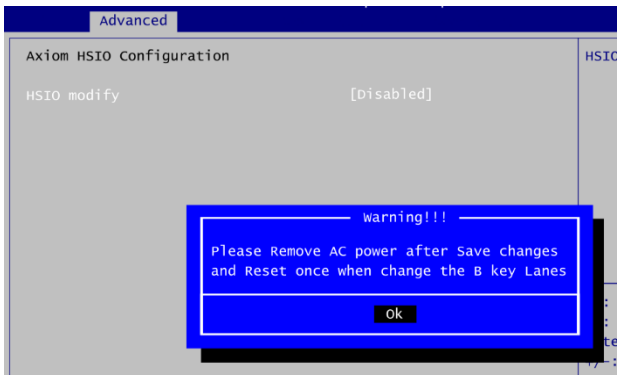


B key Configuration

The B Key can be configured to support USB+PCIE or PCIe x2. Also refer to section 2.5.18.

Note

Please remove AC power after setting and saving the configuration of B Key.

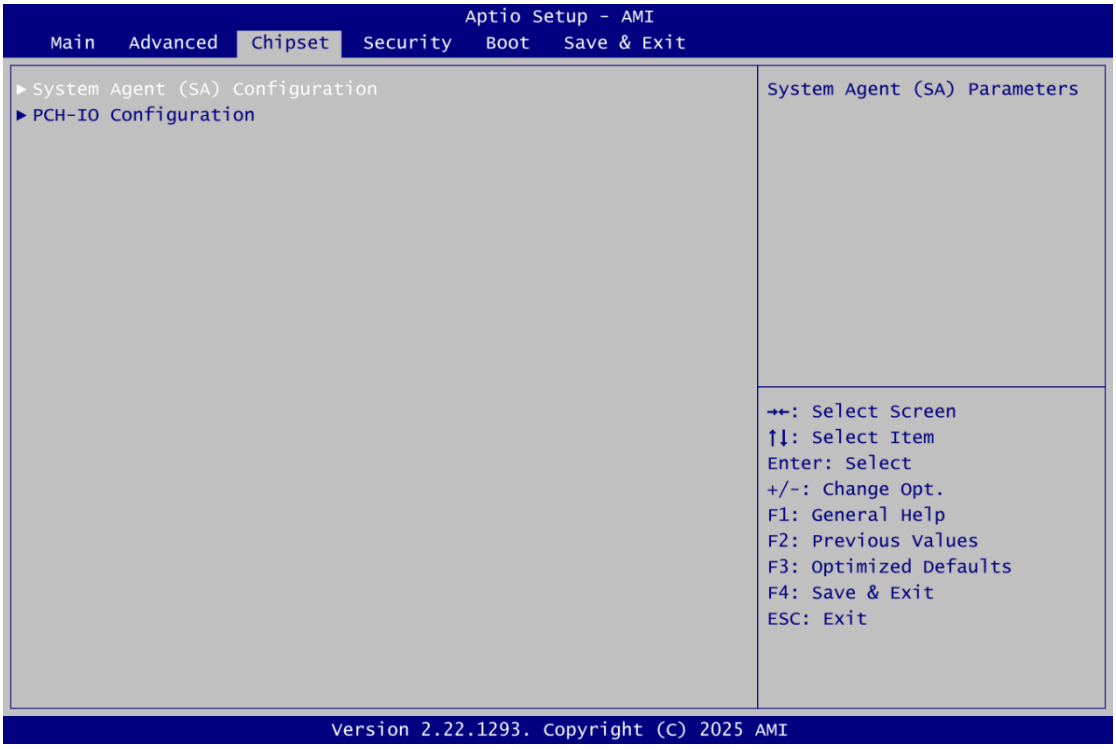


4.5 Chipset Menu

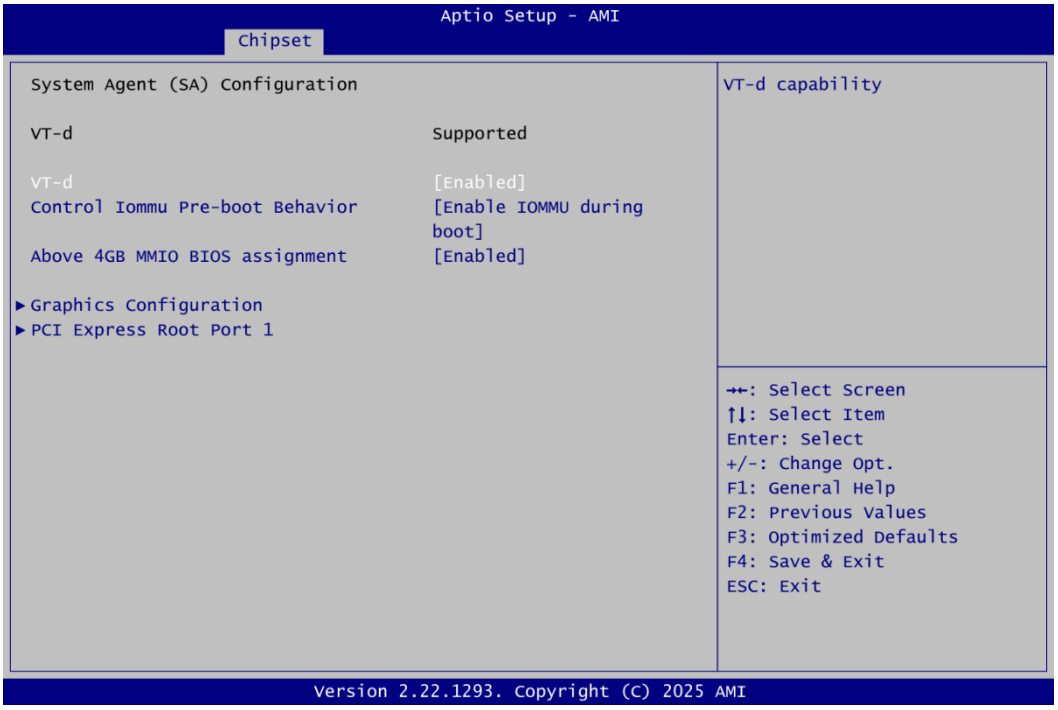
The Chipset menu allows users to change the advanced chipset settings. You can select any of the items in the left frame of the screen to go to the sub menus:

- ► System Agent (SA) Configuration
- ► PCH-IO Configuration

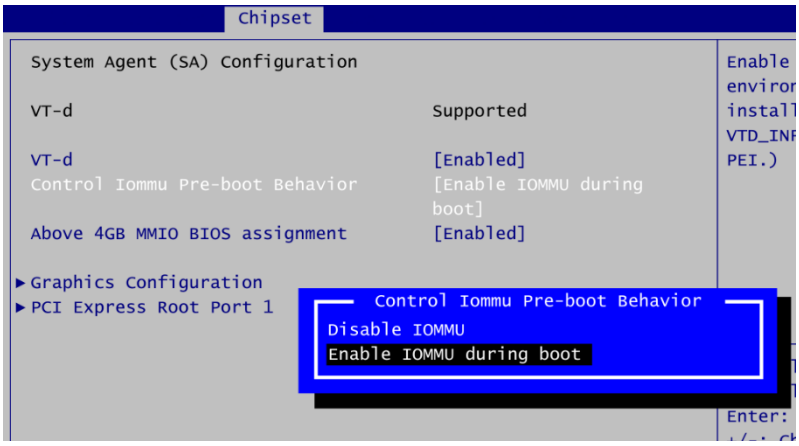
For items marked with "►", please press <Enter> for more options.



- **System Agent (SA) Configuration**
  This screen shows System Agent version information and provides function for specifying related parameters.



VT-d
Enable or disable the VT-d (Intel Virtualization Technology for Directed I/O) function. The default setting is Enabled. If this option is Disabled, the "Control IOMMU Pre-boot Behavior" setting becomes unavailable.



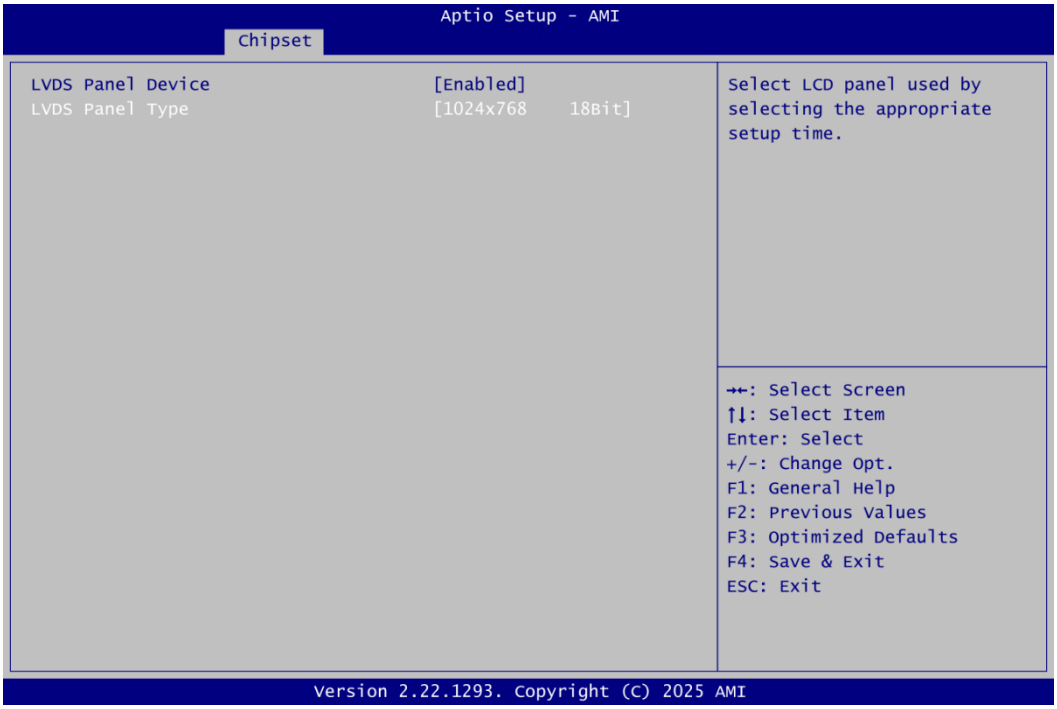
Control Iommu Pre-boot Behavior
Enable or disable the IOMMU (I/O Memory Management Unit) in pre-boot environment. Enabling it allows devices to use virtual memory addressing before the operating system loads, which is useful for virtualization and certain security features. When disable it, devices will use physical memory addressing until the operating system takes over, which may improve compatibility with legacy hardware or reduce boot complexity.

Above 4GB MMIO BIOS assignment
Enable or disable above 4GB Memory Mapped IO BIOS assignment. This is enabled automatically when Aperture Size is set to 2048MB.

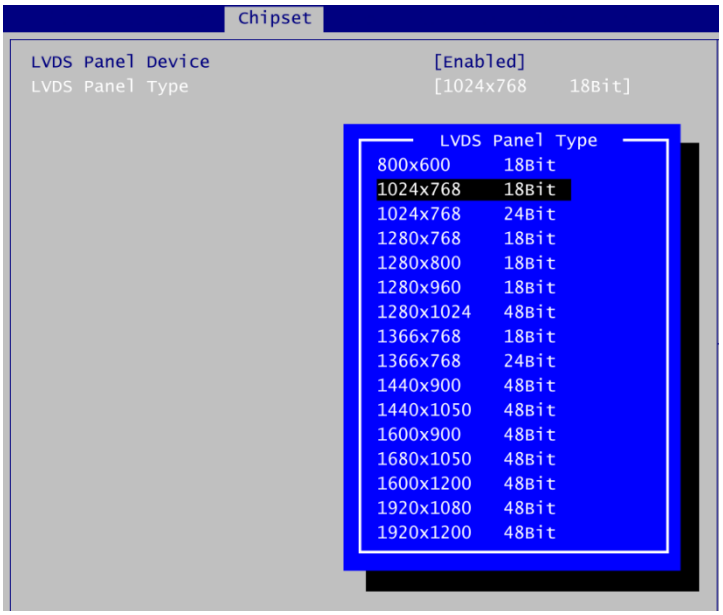
Graphics Configuration
Please press <Enter> to go to graphics configuration sub menus.

PCI Express Root Port 1
Please press <Enter> to go to PCI Express Root Port 1 settings sub menus.

- **Graphics Configuration**

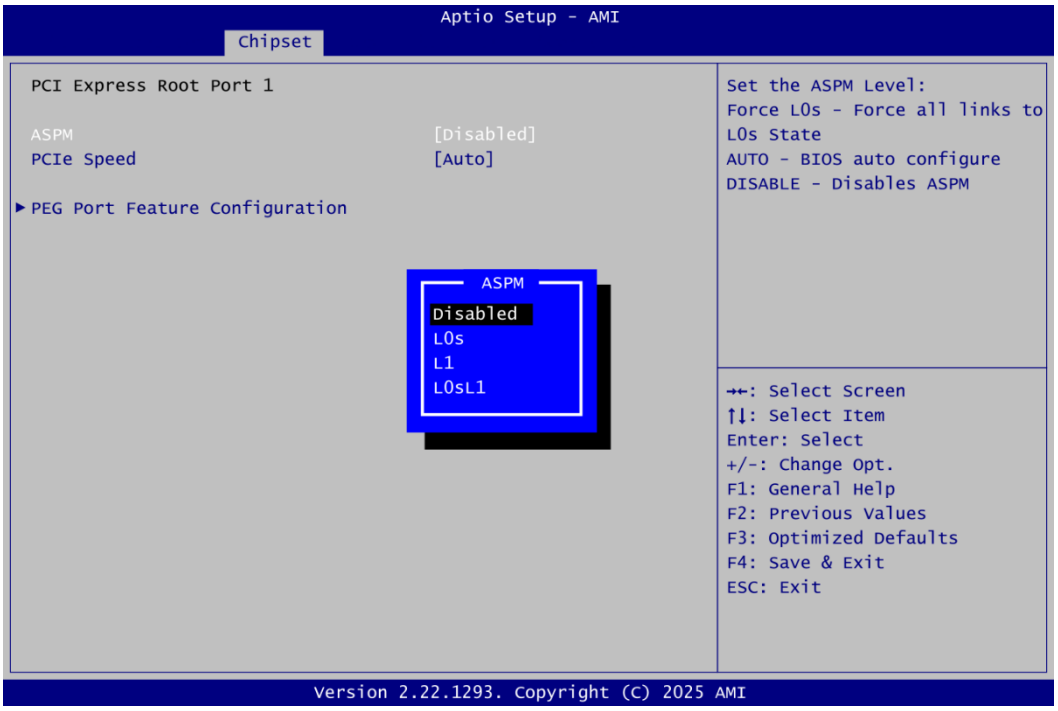


LVDS Panel Device
Enable or disable LVDS panel support.

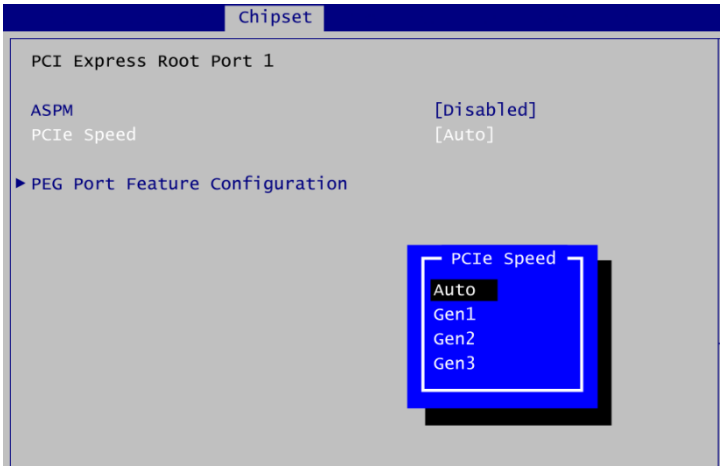


LVDS Panel Type
Select LVDS panel resolution for the display device.

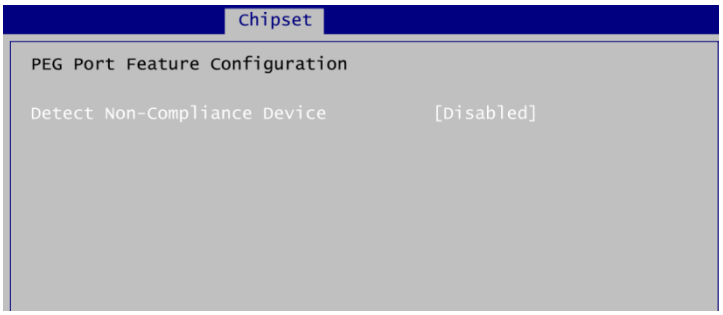
- **PCI Express Root Port 1**
  This setting configures PCIe of CN1 (see section 2.5.1).



ASPM
Sets the ASPM (Active State Power Management Settings) level.

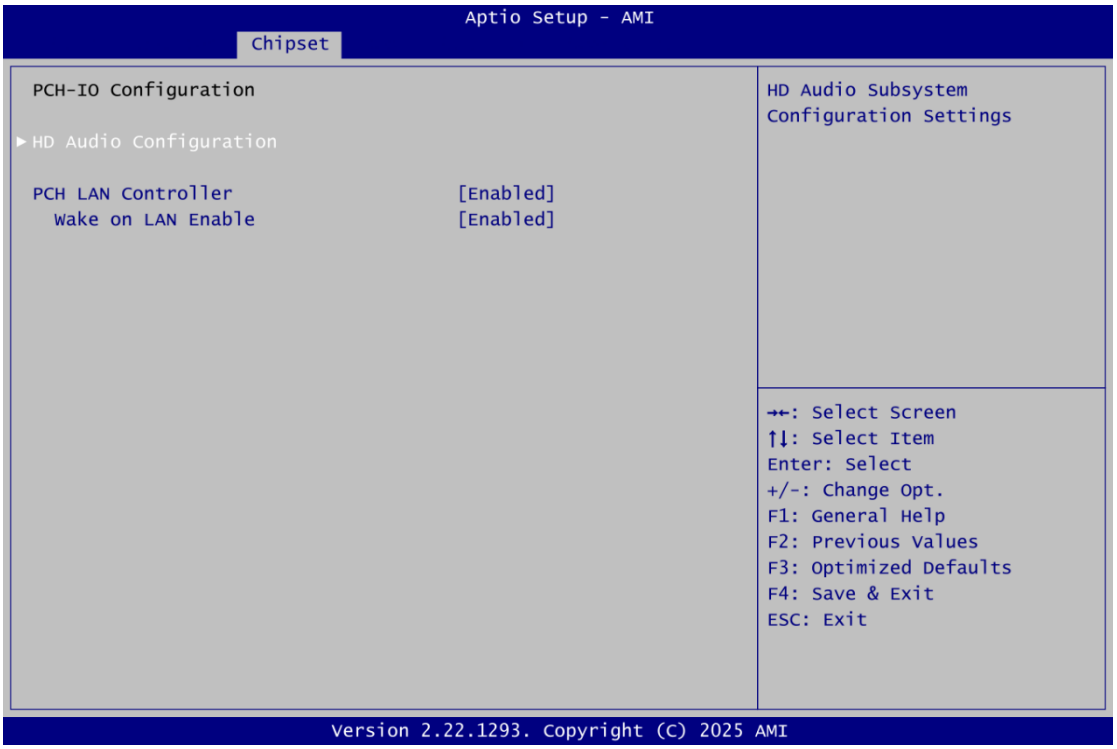


PCIe Speed
Allow user to configure PCI-Express speed.



Detect Non-Compliance Device
Enable or disable the detection of a non-compliance PCI-Express device in PEG.

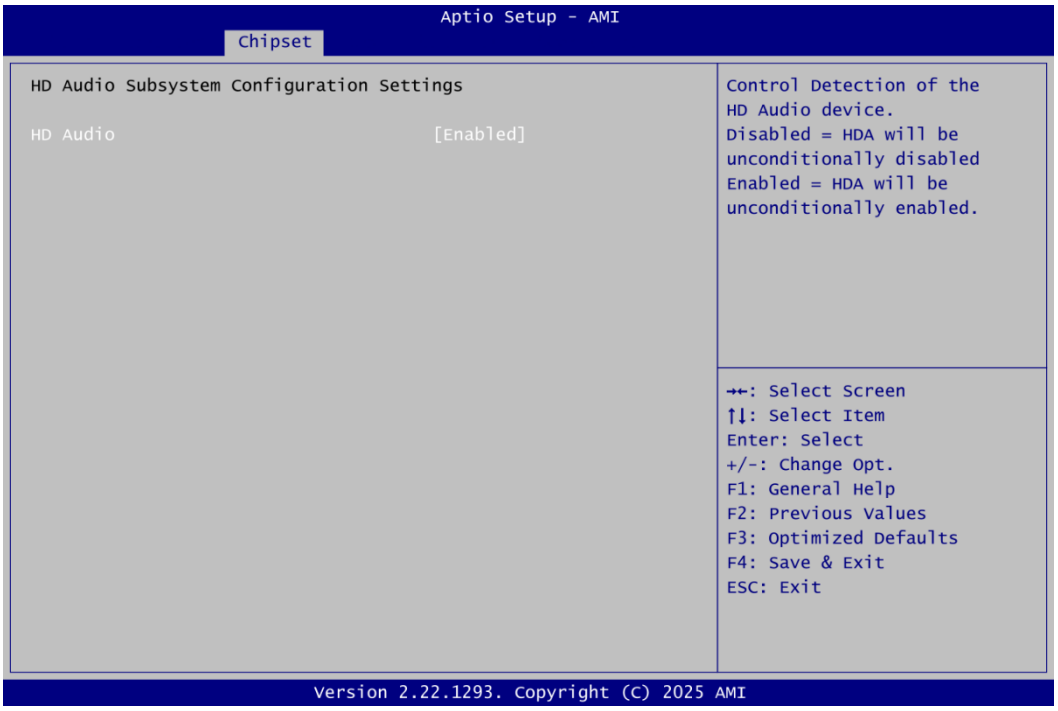
- **PCH-IO Configuration**
  This screen allows you to set PCH parameters.



PCH LAN Controller
Enable or disable onboard NIC.

Wake on LAN Enable
Enable or disable integrated LAN to wake the system.

- **HD Audio Configuration**
  HD Audio subsystem configuration settings



HD Audio
Control detection of the HD Audio device.
- Disabled: HDA will be unconditionally disabled.
- Enabled: HDA will be unconditionally enabled.

4.6 Security Menu

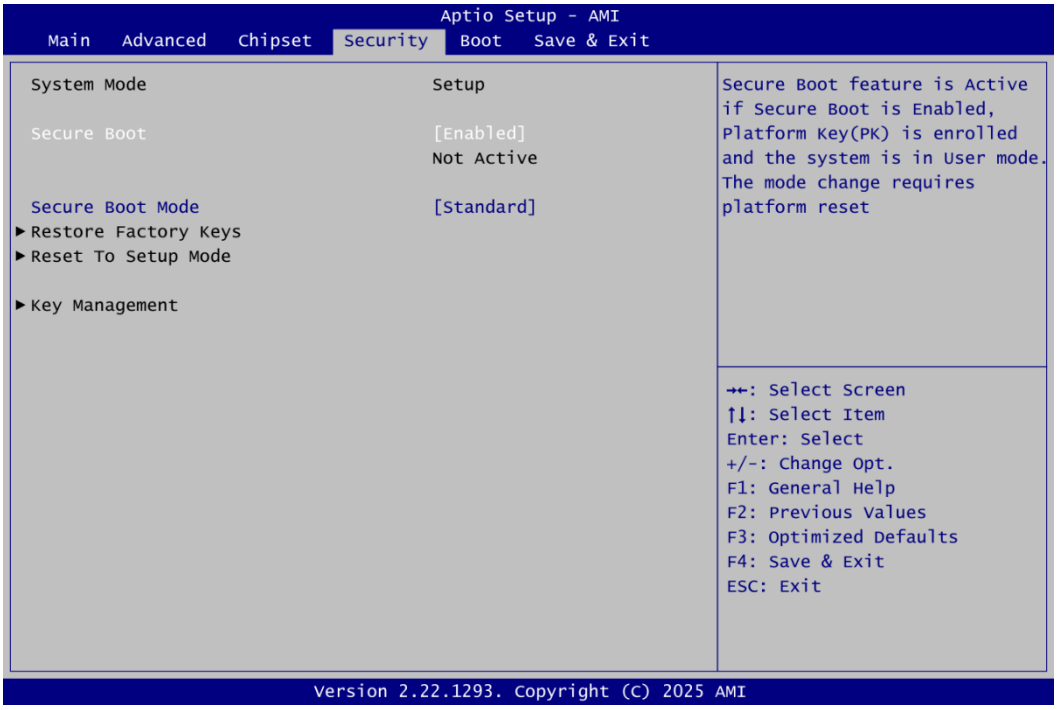
The Security menu allows users to change the security settings for the system.

- **Administrator Password**.
  Set administrator password.

- **User Password**
  Set user password.

- **Secure Boot**
  Use this item to set parameters related to Secure Boot.

- **Secure Boot**
  The Secure Boot feature is designed to ensure and protect the system from unauthorized access and malwares during boot-up.



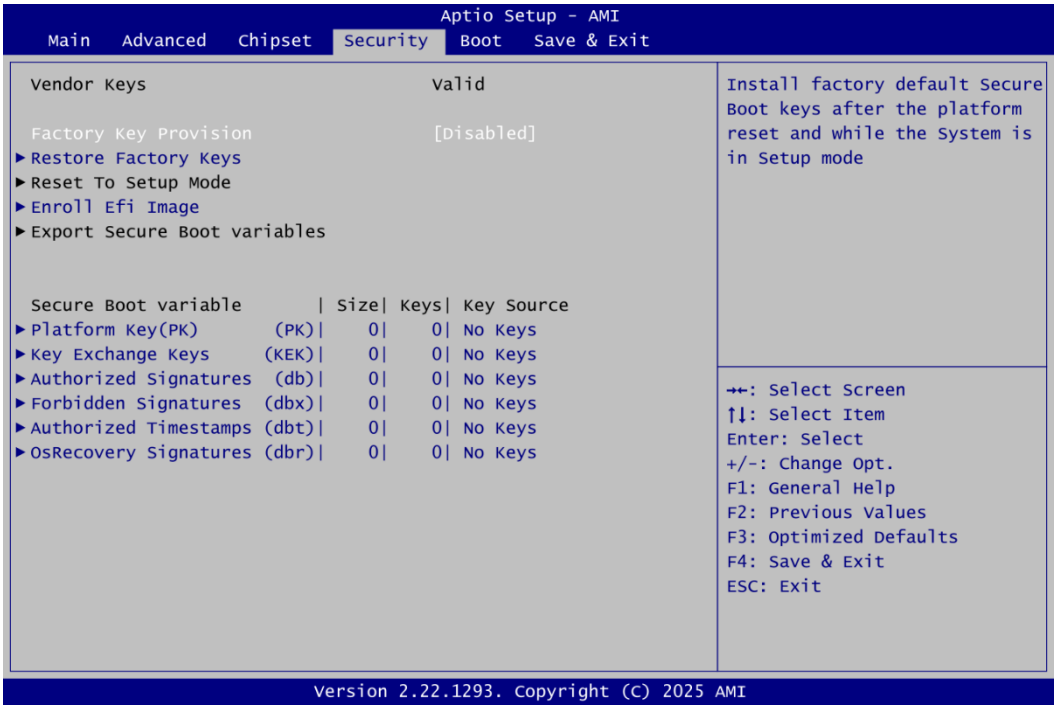
Secure Boot
Secure Boot feature is Active if Secure Boot is Enabled, Platform Key (PK) is enrolled and the System is in User mode. The mode change requires platform reset. Secure Boot ensures that the system only boots from trusted software, preventing malicious software from loading and compromising the device. It checks the digital signatures of boot loaders, firmware, and operating systems to verify that they are from trusted sources and have not been tampered with. Users can choose to enable it or not, between standard and custom mode.

Secure Boot Mode
Secure Boot mode options: Standard or Custom. In Custom mode, the policy of Secure Boot variables can be configured by a physically present user without full authentication.

Restore Factory Keys
Force System to User mode. Install factory default Secure Boot key databases.

Key Management
Enables expert users to modify Secure Boot Policy variables without full authentication.

- **Key Management**



Factory Key Provision
Enable or disable provision factory default keys on next reboot only when System in Setup mode.

Restore Factory Keys
Force System to User mode. Install factory default Secure Boot key databases.

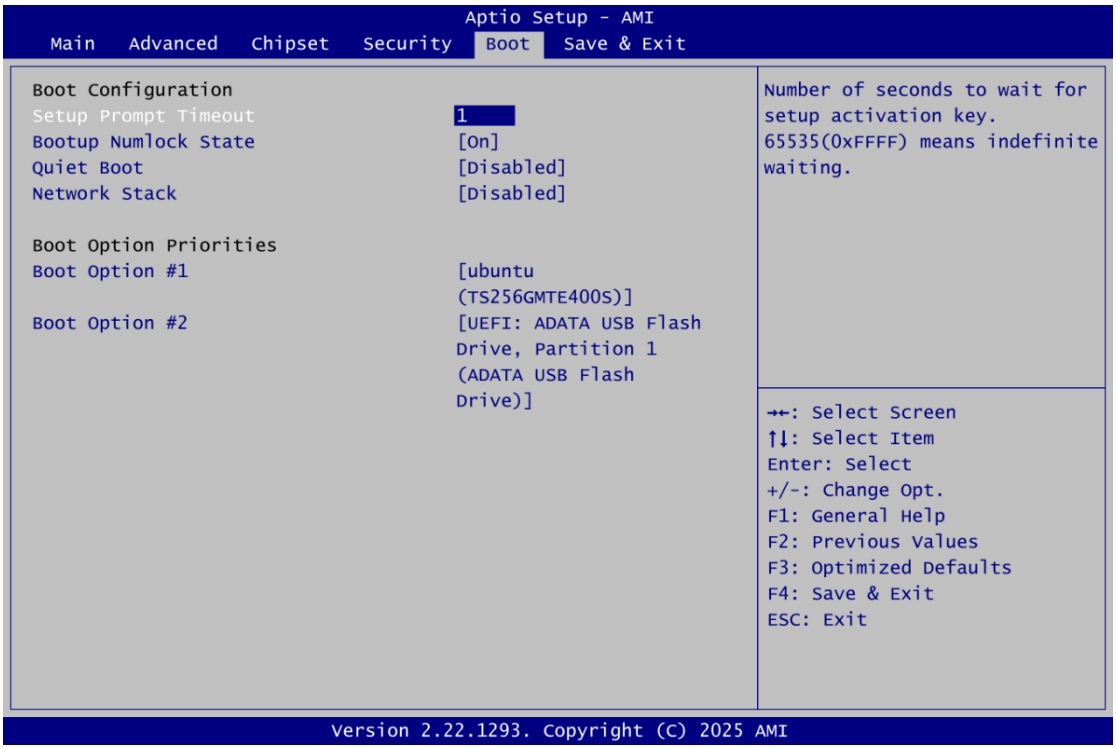
Reset To Setup Mode
Delete all Secure Boot key databases from NVRAM.

Enroll Efi Image
Allows a PE image (.efi) to run in Secure Boot mode by enrolling its SHA256 hash into the Authorized Signature Database (DB).

Export Secure Boot Variables
Export all Secure Boot variables to the files in a root folder on a file system device.

4.7 Boot Menu

The Boot menu allows users to change boot options of the system.



- **Setup Prompt Timeout**
  Number of seconds to wait for setup activation key. 65535(0xFFFF) means indefinite waiting.

- **Bootup NumLock State**
  Use this item to select the power-on state for the keyboard NumLock.

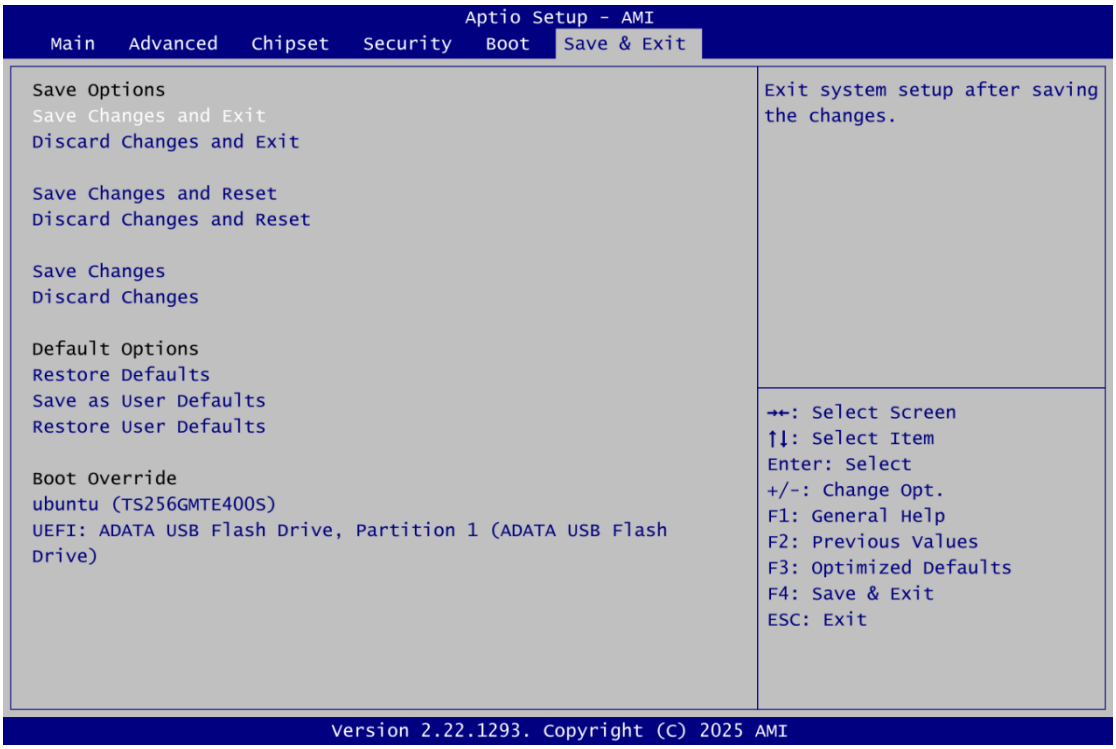
- **Quiet Boot**
  Select to display either POST output messages or a splash screen during boot-up.

- **Network Stack**
  Enable or disable UEFI Network stack.

- **Boot Option Priorities [Boot Option #1, …]**
  These are settings for boot priority. Specify the boot device priority sequence from the available devices.

4.8 Save & Exit Menu

The Save & Exit menu allows users to load your system configuration with optimal or fail-safe default values.



- **Save Changes and Exit**
  When you have completed the system configuration changes, select this option to leave Setup and return to Main Menu. Select Save Changes and Exit from the Save & Exit menu and press <Enter>. Select Yes to save changes and exit.

- **Discard Changes and Exit**
  Select this option to quit Setup without making any permanent changes to the system configuration and return to Main Menu. Select Discard Changes and Exit from the Save & Exit menu and press <Enter>. Select Yes to discard changes and exit.

- **Save Changes and Reset**
  When you have completed the system configuration changes, select this option to leave Setup and reboot the computer so the new system configuration parameters can take effect. Select Save Changes and Reset from the Save & Exit menu and press <Enter>. Select Yes to save changes and reset.

- **Discard Changes and Reset**
  Select this option to quit Setup without making any permanent changes to the system configuration and reboot the computer. Select Discard Changes and Reset from the Save & Exit menu and press <Enter>. Select Yes to discard changes and reset.

- **Save Changes**
  When you have completed the system configuration changes, select this option to save changes. Select Save Changes from the Save & Exit menu and press <Enter>. Select Yes to save changes.

- **Discard Changes**
  Select this option to quit Setup without making any permanent changes to the system configuration. Select Discard Changes from the Save & Exit menu and press <Enter>. Select Yes to discard changes.

- **Restore Defaults**
  It automatically sets all Setup options to a complete set of default settings when you select this option. Select Restore Defaults from the Save & Exit menu and press <Enter>.

- **Save as User Defaults**
  Select this option to save system configuration changes done so far as User Defaults. Select Save as User Defaults from the Save & Exit menu and press <Enter>.

- **Restore User Defaults**
  It automatically sets all Setup options to a complete set of User Defaults when you select this option. Select Restore User Defaults from the Save & Exit menu and press <Enter>.

- **Boot Override**
  Select a drive to immediately boot that device regardless of the current boot order.

Appendix A
Watchdog Timer

A.1 About Watchdog Timer

Software stability is major issue in most application. Some embedded systems are not watched by operator for 24 hours. It is usually too slow to wait for someone to reboot when computer hangs. The systems need to be able to reset automatically when things go wrong. The watchdog timer gives us solution.

The watchdog timer is a counter that triggers a system reset when it counts down to zero from a preset value. The software starts counter with an initial value and must reset it periodically. If the counter ever reaches zero which means the software has crashed, the system will reboot.

A.2 How to Use Watchdog Timer

Note

Please check Axiomtek eAPI3.0 SDK before using below sample codes.

```
//===========================================================================
//      includes
//===========================================================================

#include <stdio.h>
#include <stdlib.h>
#include <stdint.h>
#include "EApi.h"

#if defined(WIN32) || defined(_WIN32) || defined(__WIN32__) || defined(__NT__)
      #include <Windows.h>
      #include <iostream>
      #define scndata scanf_s
using namespace std;
#else
#define scndata scanf
#endif
unsigned int EapiStatus;

// ****************************************
// Watch Dog
// ****************************************
void WDT_demo()
{
   uint32_t wdt_runmode = 0;
   uint32_t wdt_timermode = 0;
   uint32_t wdt_event = 0;       // run wdt
   uint32_t wdt_delay = 0;       // run wdt
   uint32_t wdt_reset = 0;       // reload wdt

   while (wdt_runmode != 5) {
            fprintf(stderr, "1. Run WDT \n");
            fprintf(stderr, "2. Get WDT cap\n");
            fprintf(stderr, "3. Reload WDT \n");
            fprintf(stderr, "4. Stop WDT \n");
            fprintf(stderr, "5. Exit\n");
            fprintf(stderr, "Select WDT mode: ");
            scndata("%d", &wdt_runmode);

            switch (wdt_runmode)
            {
            case 1:
                     fprintf(stderr, "Set WDT timer mode (0 means second, 1 means minute):");
                     scndata("%d", &wdt_timermode);

                     if (wdt_timermode == 0)
                     {
                              fprintf(stderr, "WDT timer mode is second.\n");
                     }
                     else if (wdt_timermode == 1)
                     {
                              fprintf(stderr, "WDT timer mode is minute.\n");
                     }
                     else
                     {
                              wdt_timermode = 0;
                              fprintf(stderr, "WDT timer mode is second.\n");
                     }
```

```
                        fprintf(stderr, "Set WDT wdt_delay: ");
                        scndata("%d", &wdt_delay);

                        fprintf(stderr, "Set WDT wdt_event : ");
                        scndata("%d", &wdt_event );

                        fprintf(stderr, "Set WDT wdt_reset :");
                        scndata("%d", &wdt_reset);

                        if (wdt_timermode == 0)
                                EapiStatus = EApiWDogStart(wdt_delay * 1000, wdt_event *
1000, wdt_reset * 1000);
                        else if (wdt_timermode == 1)
                                EapiStatus = EApiWDogStart(wdt_delay * 60000, wdt_event *
60000, wdt_reset * 60000);

                        if (EapiStatus != EAPI_STATUS_SUCCESS) {
                                fprintf(stderr, "Run WDT not support!!!\n\n");
                        }
                        else {
                                fprintf(stderr, "Run WDT successful.\n\n");
                        }
                        break;
                case 2:
                        EapiStatus = EApiWDogGetCap(&wdt_delay, &wdt_event, &wdt_reset);
                        if (EapiStatus != EAPI_STATUS_SUCCESS) {
                                fprintf(stderr, "Get WDT cap not suppor!!!\n\n");
                        }
                        else {
                                fprintf(stderr, "Get WDT cap wdt_delay: %d, wdt_event: %d,
wdt_reset:%d \n\n", wdt_delay, wdt_event, wdt_reset);
                        }
                        break;
                case 3:
                        EapiStatus = EApiWDogTrigger();
                        if (EapiStatus != EAPI_STATUS_SUCCESS) {
                                fprintf(stderr, "Reload WDT not support!!!\n\n");
                        }
                        else
                                fprintf(stderr, "Reload WDT successful.\n\n");

                        break;
                case 4:
                        EapiStatus = EApiWDogStop();
                        if (EapiStatus != EAPI_STATUS_SUCCESS) {
                                fprintf(stderr, "Stop WDT not support!!!\n\n");
                        }
                        else {
                                fprintf(stderr, "Stop WDT successful.\n\n");
                        }
                        break;
                case 5:
                        fprintf(stderr, "Exit WDog mode!!!\n\n");
                        break;
                default:
                        fprintf(stderr, "Select error!!!\n\n");
                        break;
                }
                fprintf(stderr, "*****************************************\n");
                }
```

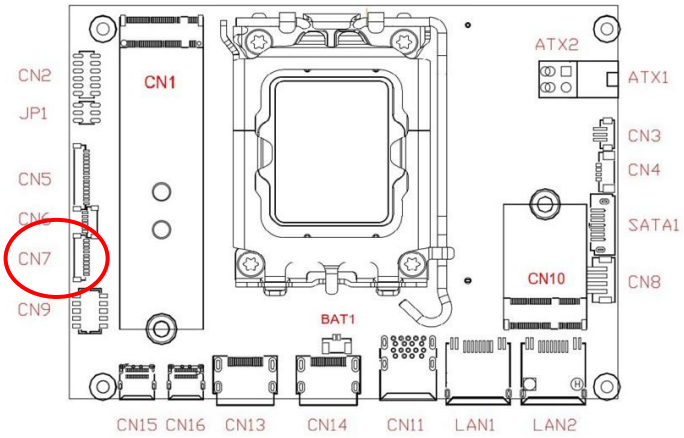
```
}

int main (
        int argc,
        char *argv[]
) {
        //
        // Initialize
        //
        EapiStatus = EApiLibInitialize ();
        if (EapiStatus != EAPI_STATUS_SUCCESS) {
                fprintf (stderr, "Fail to initialize");
        }
        else
        {
                fprintf (stderr, "---- intialize: ok\n");
                WDT_demo();
        }
        return 0;
}
```

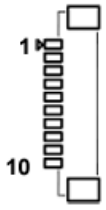
Appendix B
Digital I/O

B.1 About Digital I/O

The digital I/O on CPU board has 8 bits. Each bit can be set to function as input or output by software programming. In default, all pins are pulled high with +5V level (according to main power). The BIOS default settings are 8 inputs where all of these pins are set to 1.



CN7



Pin	Signal	Pin	Signal
1	DIO0	6	DIO5
2	DIO7	7	DIO3
3	DIO1	8	DIO4
4	DIO6	9	+5V
5	DIO2	10	GND

Note

The maximum current @5V is up to 85mA. Each DO can be up to 10mA at least.

B.2 Digital I/O Programming

Note

Please check Axiomtek eAPI3.0 SDK before using below sample codes.

```
#include <stdio.h>
#include <stdlib.h>
#include <stdint.h>
#include "EApi.h"
#if defined(WIN32) || defined(_WIN32) || defined(__WIN32__) || defined(__NT__)
	#include <Windows.h>
	#include <iostream>
	#define scndata scanf_s
using namespace std;

#else

#define scndata scanf

#endif
unsigned int EapiStatus;
// ****************************************
// Menu
// ****************************************


// ****************************************
// Load and Initilize eAPI library
// ****************************************
int InitLibrary()
{

	return EApiLibInitialize() != EAPI_STATUS_SUCCESS;
}

void GPIO_demo()
{
	uint32_t GPIO_runmode = 0;
	uint32_t ID = 0;
	uint32_t mask = 0;
	uint32_t value = 0;
	uint32_t inmask = 0;

	while (GPIO_runmode != 6) {
		ID = 0;
		mask = 0;
		value = 0;
		inmask = 0;
		fprintf(stderr, "1. Get GPIO DirectionCaps\n");
		fprintf(stderr, "2. Get GPIO Direction\n");
		fprintf(stderr, "3. Set GPIO Direction\n");
		fprintf(stderr, "4. Get GPIO Level\n");
		fprintf(stderr, "5. Set GPIO Level\n");
		fprintf(stderr, "6. Exit\n");
```

```
		fprintf(stderr, "Select GPIO run mode: ");
		scndata("%d", &GPIO_runmode);
		switch (GPIO_runmode)
		{
		case 1:
			fprintf(stderr, "Bank: 0x10000\n");
			fprintf(stderr, "Enter the ID(hex): ");
			scndata("%x", &ID);
			EapiStatus = EApiGPIOGetDirectionCaps(ID, &mask, &value);
			if (EapiStatus != EAPI_STATUS_SUCCESS) {
				fprintf(stderr, "Get GPIO DirectionCaps not support!!!\n\n");
			}
			else {
				fprintf(stderr, "Get GPIO DirectionCaps ID: %x, Inputmask: %x,
Outputmask: %x\n\n", ID, mask, value);
			}
			break;
		case 2:
			fprintf(stderr, "Bank: 0x10000\n");
			fprintf(stderr, "Enter the ID(hex): ");
			scndata("%x", &ID);
			fprintf(stderr, "Enter the mask(hex): ");
			scndata("%x", &mask);
			EapiStatus = EApiGPIOGetDirection(ID, mask, &value);
			if (EapiStatus != EAPI_STATUS_SUCCESS) {
				fprintf(stderr, "Get GPIO Direction not support!!!\n\n");
			}
			else {
				fprintf(stderr, "Get GPIO Direction ID: %x, mask: %x, Direction:
%x\n\n", ID, mask, value);
			}
			break;
		case 3:
			fprintf(stderr, "Bank: 0x10000\n");
			fprintf(stderr, "Enter the ID(hex): ");
			scndata("%x", &ID);
			fprintf(stderr, "Enter the mask(hex): ");
			scndata("%x", &mask);
			fprintf(stderr, "Enter the Direction(hex): ");
			scndata("%x", &value);
			EapiStatus = EApiGPIOSetDirection(ID, mask, value);
			if (EapiStatus != EAPI_STATUS_SUCCESS) {
				fprintf(stderr, "Set GPIO Direction not support!!!\n\n");
			}
			else {
				fprintf(stderr, "Set GPIO Direction successful\n\n");
			}
			break;
		case 4:
			fprintf(stderr, "Bank: 0x10000\n");
			fprintf(stderr, "Enter the ID(hex): ");
			scndata("%x", &ID);
			fprintf(stderr, "Enter the mask(hex): ");
			scndata("%x", &mask);
			EapiStatus = EApiGPIOGetLevel(ID, mask, &value);
			if (EapiStatus != EAPI_STATUS_SUCCESS) {
				fprintf(stderr, "Get GPIO Level not support!!!\n\n");
			}
			else {
```

```
                                        fprintf(stderr, "Get GPIO Level ID: %x, mask: %x, Level: %x\n\n",
ID, mask, value);
                        }
                        break;
                case 5:
                        fprintf(stderr, "Bank: 0x10000\n");
                        fprintf(stderr, "Enter the ID(hex): ");
                        scndata("%x", &ID);
                        fprintf(stderr, "Enter the mask(hex): ");
                        scndata("%x", &mask);
                        fprintf(stderr, "Enter the Level(hex): ");
                        scndata("%x", &value);
                        EapiStatus = EApiGPIOSetLevel(ID, mask, value);
                        if (EapiStatus != EAPI_STATUS_SUCCESS) {
                                fprintf(stderr, "Set GPIO Level not support!!!\n\n");
                        }
                        else {
                                fprintf(stderr, "Set GPIO Level successful\n\n");
                        }
                        break;
                        break;
                case 6:
                        fprintf(stderr, "Exit program!!!\n\n");
                        break;
                default:
                        fprintf(stderr, "GPIO error!!!\n\n");
                        break;
                }
                fprintf(stderr, "*****************************************\n");
                }
}


// ****************************************
// Main
// ****************************************
int main()
{
      int select = 0;

      if (InitLibrary() != 0)
      {
            fprintf(stderr,"---- intialize: fail\n");
            // system("pause");
            return 1;
      }
            fprintf(stderr, "---- intialize: ok\n");
            GPIO_demo();
      // system("pause");
      return 0;
}
```