



AXIOMTEK

Q7M100

**Freescale i.MX28 Series ARM-based
Qseven System-on-Module**

Hardware User's Manual



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CAUTION

If you replace wrong batteries, it causes the danger of explosion. It is recommended by the manufacturer that you follow the manufacturer's instructions to only replace the same or equivalent type of battery, and dispose of used ones.

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ESD Precautions

Computer boards have integrated circuits sensitive to static electricity. To prevent chipsets from electrostatic discharge damage, please take care of the following jobs with precautions:

- Do not remove boards or integrated circuits from their anti-static packaging until you are ready to install them.
- Before holding the board or integrated circuit, touch an unpainted portion of the system unit chassis for a few seconds. It discharges static electricity from your body.
- Wear a wrist-grounding strap, available from most electronic component stores, when handling boards and components.

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Chapter 1

Introduction



The Q7M100 is a new Qseven module to support Freescale i.MX28 series SoCs. It integrates system memory, storage as eMMC/SDHC socket, TTL LCD, audio, USB host/client, UARTs, CANBus and various I/O features. Taking the low power consumption advantages of ARM RISC architecture, the Q7M100 is extremely suitable to be deployed in the deeply embedded applications; such as HMI, data logger, extended temperature embedded controllers, etc.

1.1 Features

- Freescale i.MX28 family SoC information:

Feature	i.MX283	i.MX286	i.MX287
On-chip RAM	128KB	128KB	128KB
Memory I/F	NAND Flash, DDR2, mDDR, LV-DDR2	NAND Flash, DDR2, mDDR, LV-DDR2	NAND Flash, DDR2, mDDR, LV-DDR2
LCD Interface	Yes	Yes	Yes
Touchscreen	Yes	Yes	Yes
Ethernet	x1	x1	x2
L2 Switch	-	-	Yes
CAN	-	x2	x2
12-bit ADC	x8	x8	x8
High Speed ADC	x1	x1	x1
USB 2.0	OTG HS with HS PHY x1 HS Host with HS PHY x1	OTG HS with HS PHY x1 HS Host with HS PHY x1	OTG HS with HS PHY x1 HS Host with HS PHY x1
SDIO	x1	x1	x1
SPI	x1	x1	x1
UART	x4	x4	x4
PWM	Built-in	Built-in	Built-in
S/PDIF Tx	-	Yes	Yes
Package	14x14 0.8mm 289 BGA	14x14 0.8mm 289 BGA	14x14 0.8mm 289 BGA

- Onboard DDR2-667 memory supports up to 128MB capacity
- Onboard eMMC flash as booting device
- 24-bit TTL LCD
- 2 USB 2.0 ports
- 2 100/10 Base-T Ethernet
- IIS Audio

1.2 Specifications

- **CPU**
 - Freescale i.MX28 series SoC; default is i.MX287.
 - ARM926EL-S CPU running at 454MHz.
 - 128KB integrated low power on-chip SRAM.
 - 128KB integrated mask-programmable on-chip ROM.
 - 1280 bits of on-chip one-time-programmable (OCOTP) ROM.
- **Boot ROM**
 - Linux kernel 2.6.35 and Windows CE 6.0.
(Please contact your agent for detail shipping content).
- **System Memory**
 - Maximum up to 128MB DDR2-667 memory.
- **USB Interface**
 - Two USB 2.0 ports comply with USB Spec. Rev. 2.0.
 - One USB port OTG client controller and PHY; and one USB 2.0 host controller and PHY.
- **Storage Interface**
 - One eMMC flash chip on module with up to 20-bit BCH ECC; default is 4GB.
- **Display**
 - Controller integrated into Freescale i.MX28 SoC.
 - Support LCD output interface as maximum 24-bit RGB (DOTCK) modes and 24-bit system-mode TTL LCD.
 - Pixel-processing pipeline (PXP) supports full path from color-space conversion, scaling, alpha-blending to rotation without intermediate memory access.
- **Ethernet**
 - Two 100/10 Base-T with Freescale i.MX28 integrated MAC and SMSC LAN8720A PHY.
 - Compatible with IEEE std 802.3.
 - Support IEEE std 1588-compatible hardware timestamp.
 - Support 50MHz/25MHz clock output for external PHY.
- **Audio**
 - Freescale IIS SGTL5000 codec for MIC-in/headphone via Qseven MXM interface.
- **Serial Port**
 - Support up to four (two as TX/RX/RTS/CTS and two as TX/RX) UARTs up to 3.25Mbps (RS-422/485 only) with hardware flow control.
 - Two RS-232 and one RS-422/485, one TX/RX 3.3V TTL to be transmitted on the baseboard.
- **CANBus**
 - Two 2.0B protocol-compatible Controller Area Network (CAN) interface.
 - One via Qseven MXM interface, one via Axiomtek ZIF connector.
- **I²C**
 - Two I²C Master/Slave interfaces (up to 400kbps) connected to Qseven MXM interface.

- **SPI**
 - One SPI channel for 2 chip select via Qseven MXM interface.
- **GPIO**
 - Eight GPIO interfaces (up to 400kbps) wired to Axiomtek ZIF connector.
- **Other I/Os**
 - 6-channel low resolution A/D converter (LRADC), touch screen signals (4/5-wire touchscreen controller) included via Axiomtek ZIF connector.
 - Eight keypad matrix with button-detect circuit routed to Axiomtek ZIF connector.
- **Power**
 - +5V \pm 5% DC-in.
- **Form Factor**
 - 70mm x 70mm.
 - Thickness as 1.2mm \pm 0.1mm.
 - Qseven specifications v1.2 compliant.
- **Environments**
 - Operating temperature: -40 ~ 85°C (system with 20cm/sec airflow in the surface).
 - Operating humidity: 10% RH ~ 95% RH relative humidity, non-condensing.

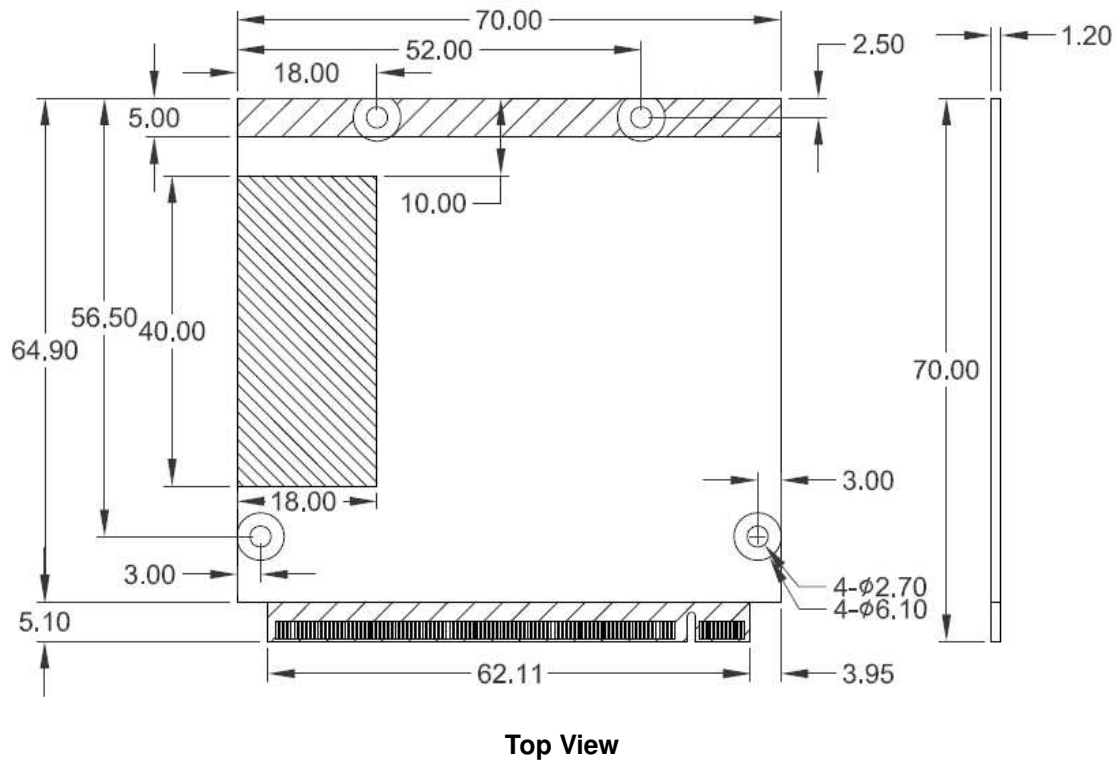


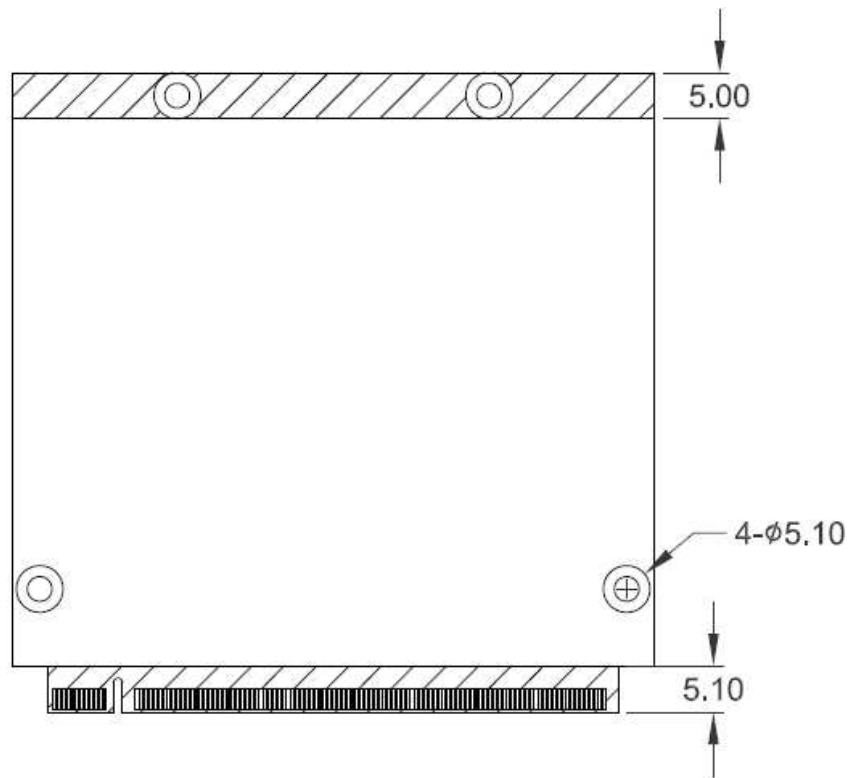
Note: *All specifications and images are subject to change without notice.*

Chapter 2

Board and Pin Assignments

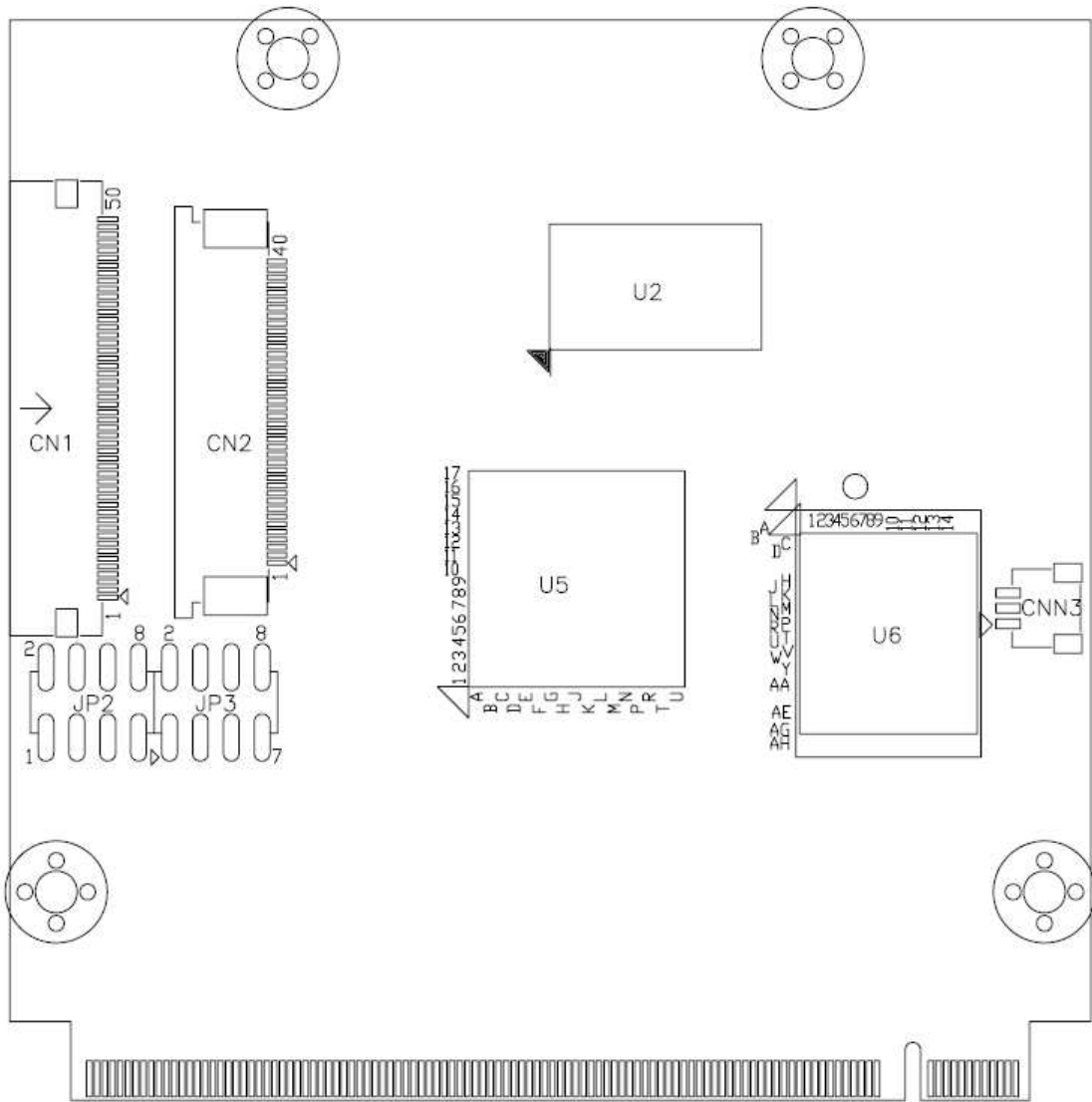
2.1 Board Dimensions and Fixing Holes



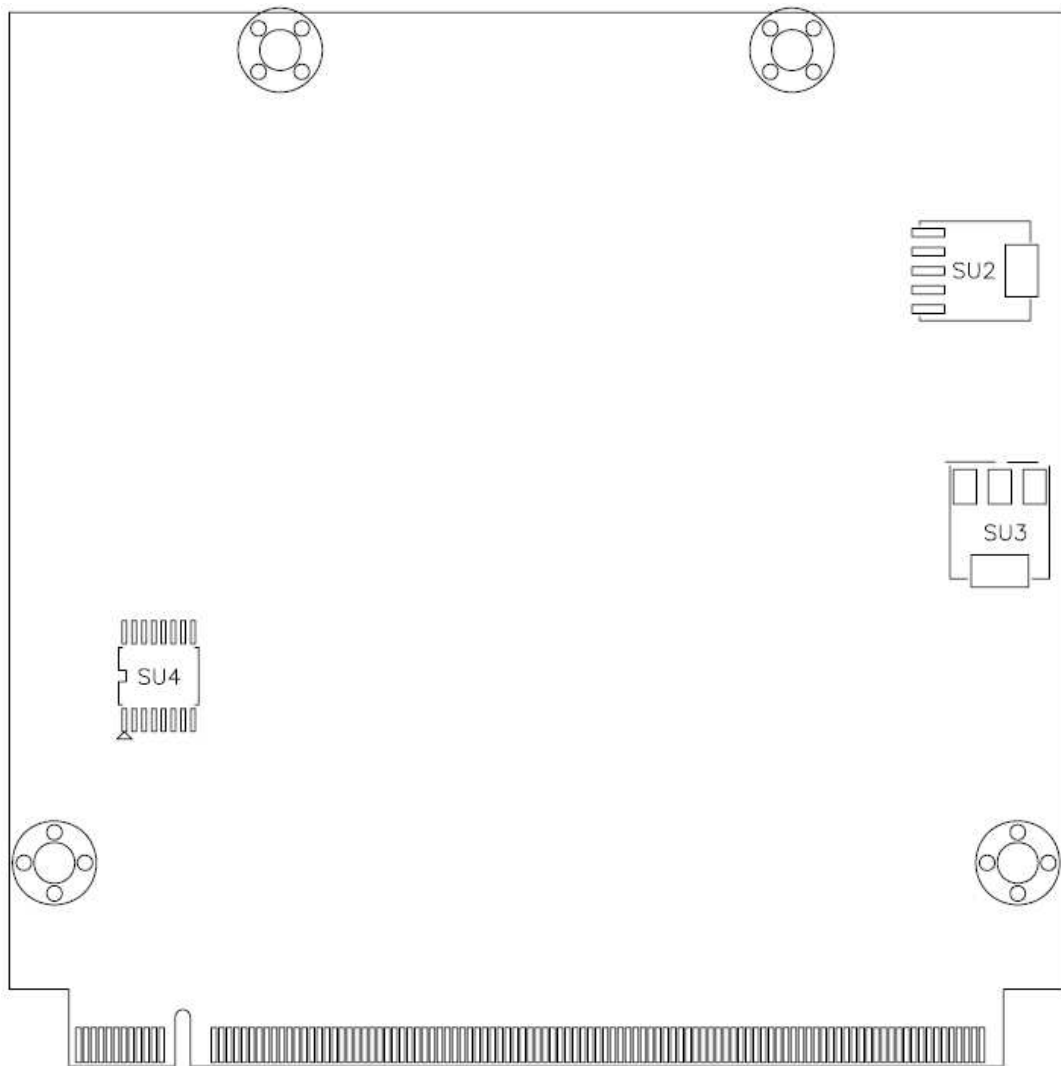


Bottom View

2.2 Board Layout



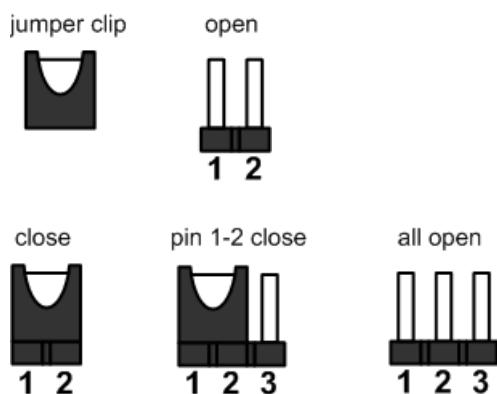
Top View



Bottom View

2.3 Jumper Settings

Jumper is a small component consisting of jumper clip and jumper pins. Install jumper clip on 2 jumper pins to close. And remove jumper clip from 2 jumper pins to open. Below illustration shows how to set up jumper.



Properly configure jumpers on the Q7M100 to meet your application purpose. Below you can find a summary table of all jumpers and onboard default setting.



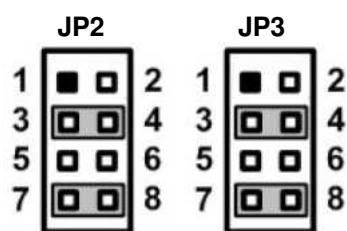
Note: Once the default jumper setting needs to be changed, please do it under power-off condition.

Jumper	Description	Setting
JP2	Boot Mode Selection	3-4, 7-8 Close
JP3	Default: Copy image to eMMC	3-4, 7-8 Close

2.3.1 Boot Mode Selection (JP2 and JP3)

These jumpers are for boot mode selection.

Function	Setting
Copy image to eMMC (Default)	JP2 3-4, 7-8 close JP3 3-4, 7-8 close
Boot to OS	JP2 1-2, 7-8 close JP3 3-4, 5-6 close



2.4 Connectors

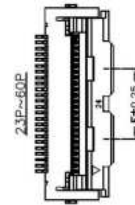
Signals go to other parts of the system through connectors. Loose or improper connection might cause problems, please make sure all connectors are properly and firmly connected. Here is a summary table which shows all connectors on the hardware.

Connector	Description
CN1	50-pin ZIF Connector for Axiomtek Proprietary IO
CN2	40-pin ZIF Connector for TTL LCD
CNN3	Debug Port Connector

2.4.1 ZIF Connectors (CN1 and CN2)

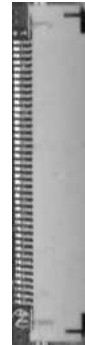
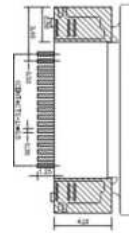
This board has a 50-pin ZIF connector (CN1) for interfacing Axiomtek Proprietary IO to baseboard.

Pin	Signal	Pin	Signal
1	GND	2	GPIO3_27
3	GPIO2_14	4	GPIO1_30
5	GPIO1_29	6	GPIO1_28
7	GPIO0_27	8	GPIO0_26
9	GPIO0_24	10	GPIO0_17
11	GPIO0_16	12	USB1_PWR_EN
13	USB0_PWR_EN	14	CAN_PWDN
15	GND	16	HSADC0
17	GND	18	LRADC1
19	GND	20	LRADC6
21	GND	22	LRADC3
23	GND	24	LRADC5
25	GND	26	LRADC2
27	GND	28	LRADC4
29	GND	30	CAN1_RX
31	CAN1_TX	32	GND
33	COM3_TX	34	GPIO2_26
35	COM3_RX	36	N.C.
37	GND	38	COM2_CTS
39	COM2_RX	40	COM2_RTS
41	COM2_TX	42	GND
43	COM1_CTS	44	COM1_RX
45	COM1_RTS	46	COM1_TX
47	GND	48	COM4_TX
49	COM4_RX	50	GND



This board also has a 40-pin ZIF connector (CN2) for interfacing TTL LCD to baseboard.

Pin	Signal	Pin	Signal
1	GND	2	GND
3	N.C.	4	N.C.
5	LCD_D16	6	LCD_D17
7	LCD_D18	8	LCD_D19
9	LCD_D20	10	LCD_D21
11	LCD_D22	12	LCD_D23
13	LCD_D08	14	LCD_D09
15	LCD_D10	16	LCD_D11
17	LCD_D12	18	LCD_D13
19	LCD_D14	20	LCD_D15
21	LCD_D00	22	LCD_D01
23	LCD_D02	24	LCD_D03
25	LCD_D04	26	LCD_D05
27	LCD_D06	28	LCD_D07
29	GND	30	LCD_CLOCKIN
31	LCD_DISP	32	LCD_HSYNC
33	LCD_VSYNC	34	LCD_ENABLE
35	N.C.	36	N.C.
37	GND	38	GND
39	N.C.	40	N.C.



2.4.2 Debug Port Connector (CNN3)

The CNN3 is a 3-pin wafer connector for TX/RX debug UART port, see table below.

Pin	Signal
1	Debug TX
2	Debug RX
3	GND



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